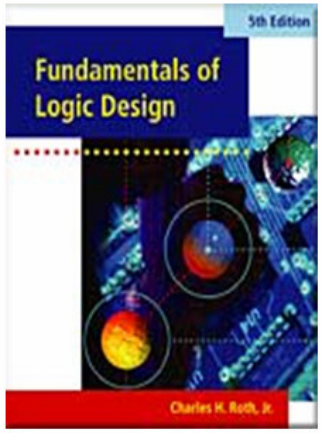
FIGURES FOR

CHAPTER 8

COMBINATIONAL CIRCUIT DESIGN AND SIMULATION USING GATES



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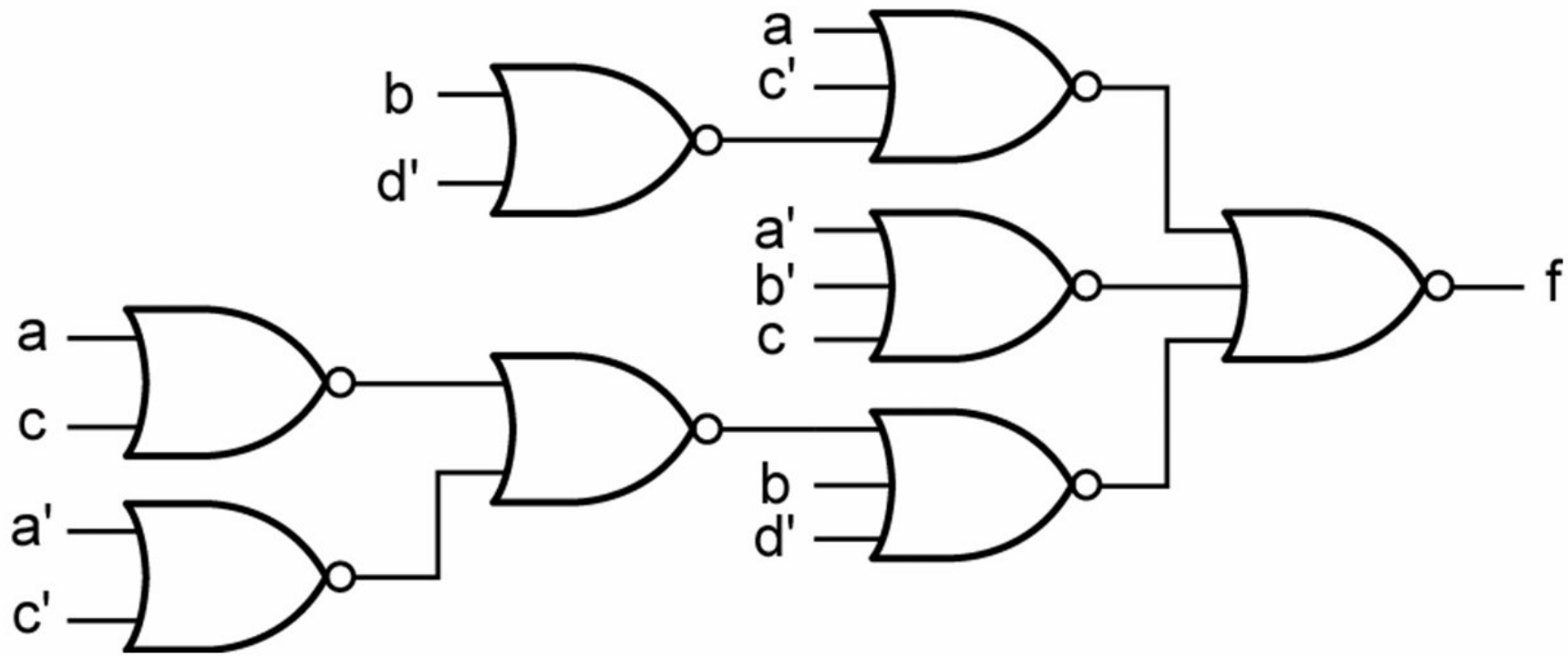
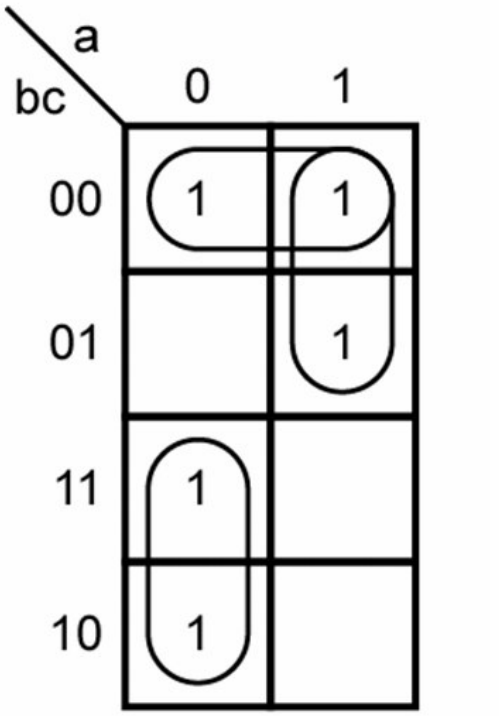
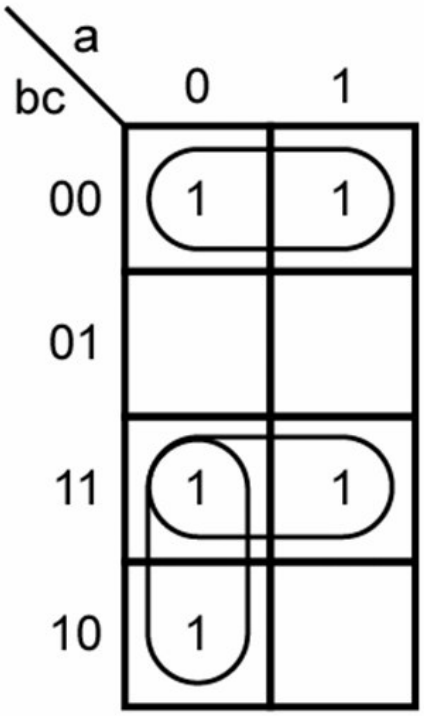


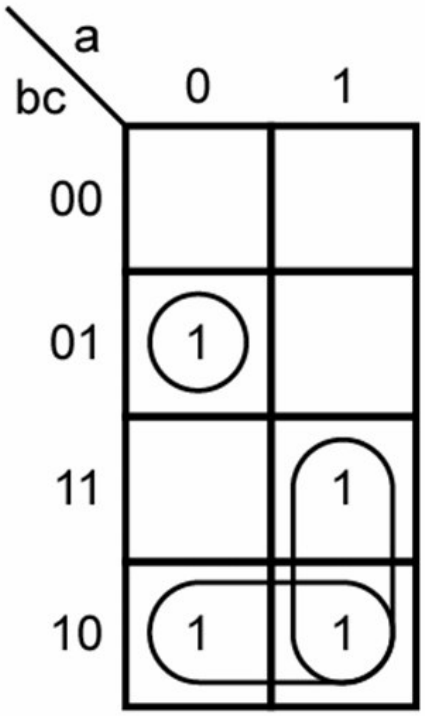
Figure 8-1



$f_1 = \Sigma m\ (0, 2, 3, 4, 5)$



$f_2 = \Sigma m\ (0, 2, 3, 4, 7)$



$f_3 = \Sigma m\ (1, 2, 6, 7)$

Figure 8-2

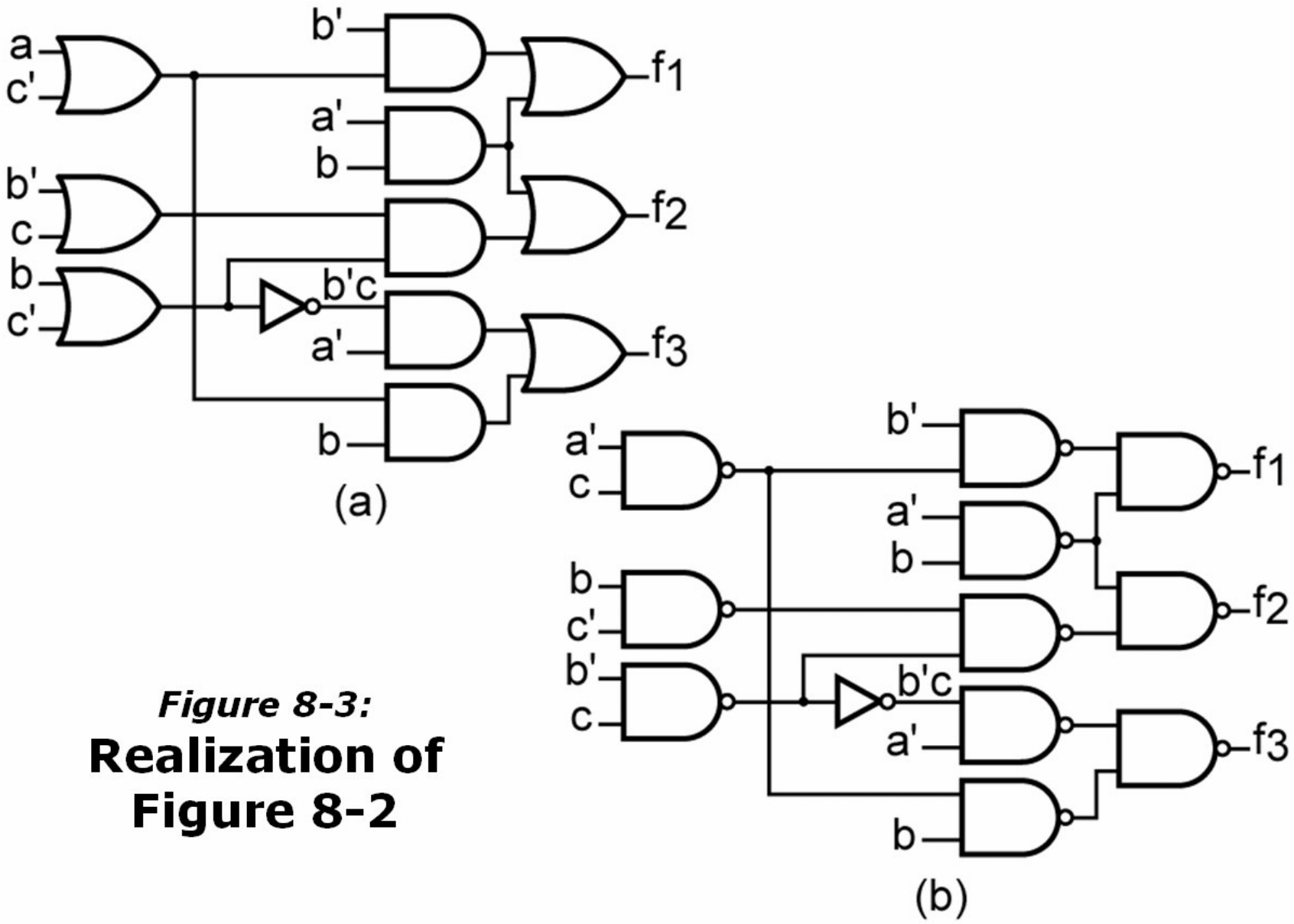


Figure 8-3:

Realization of Figure 8-2

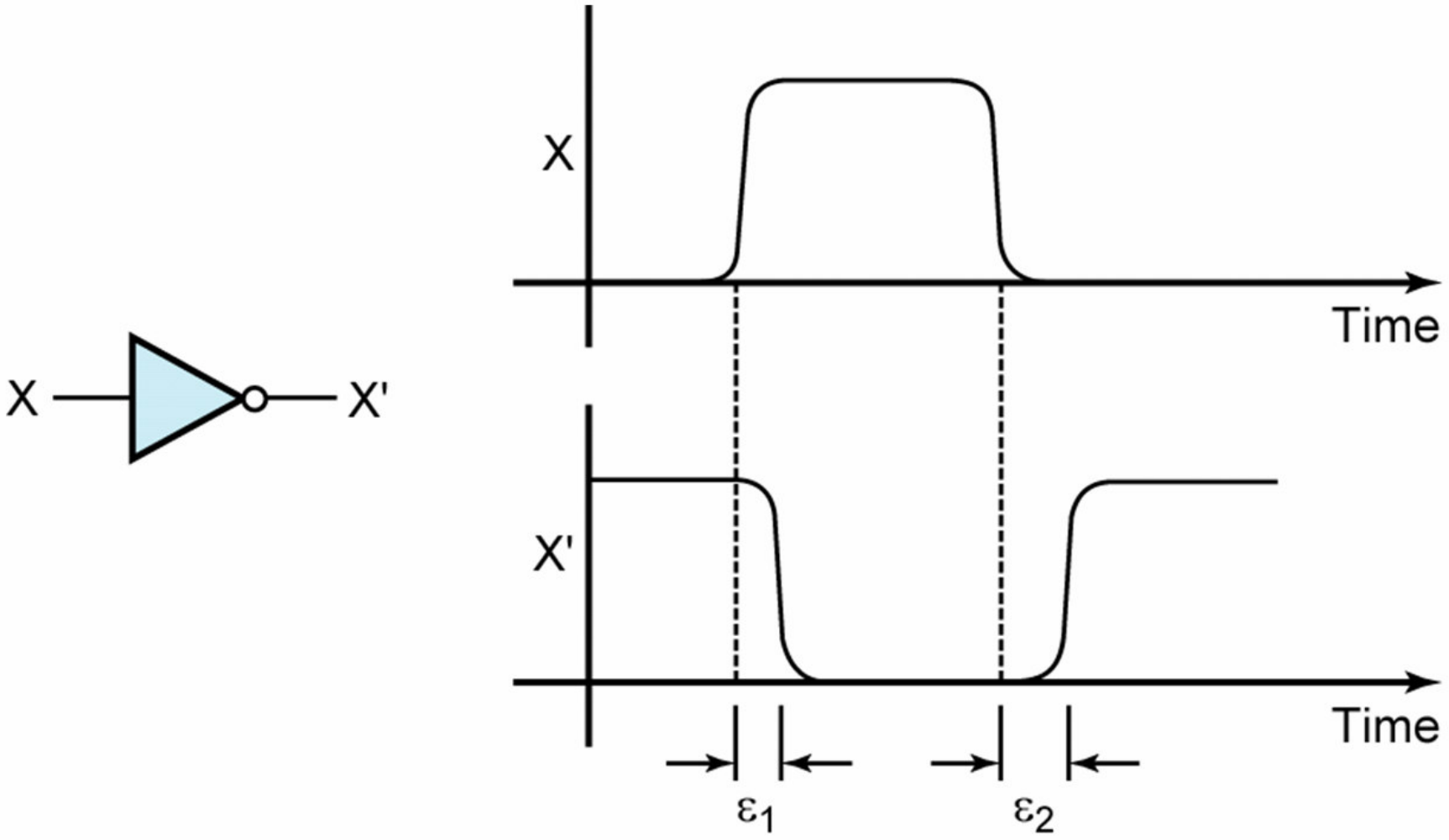


Figure 8-4: **Propagation Delay in an Inverter**

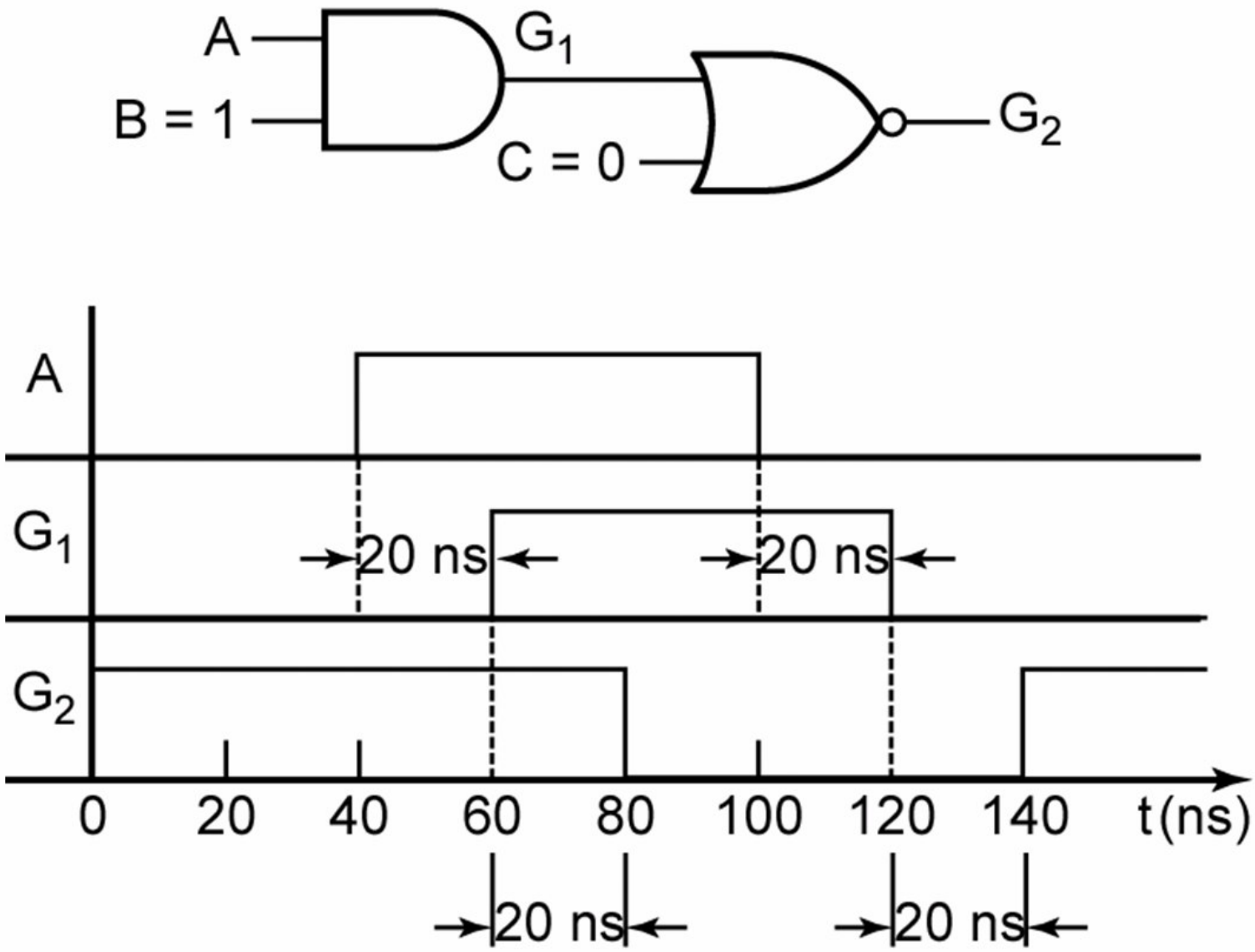


Figure 8-5: **Timing Diagram for AND-NOR Circuit**

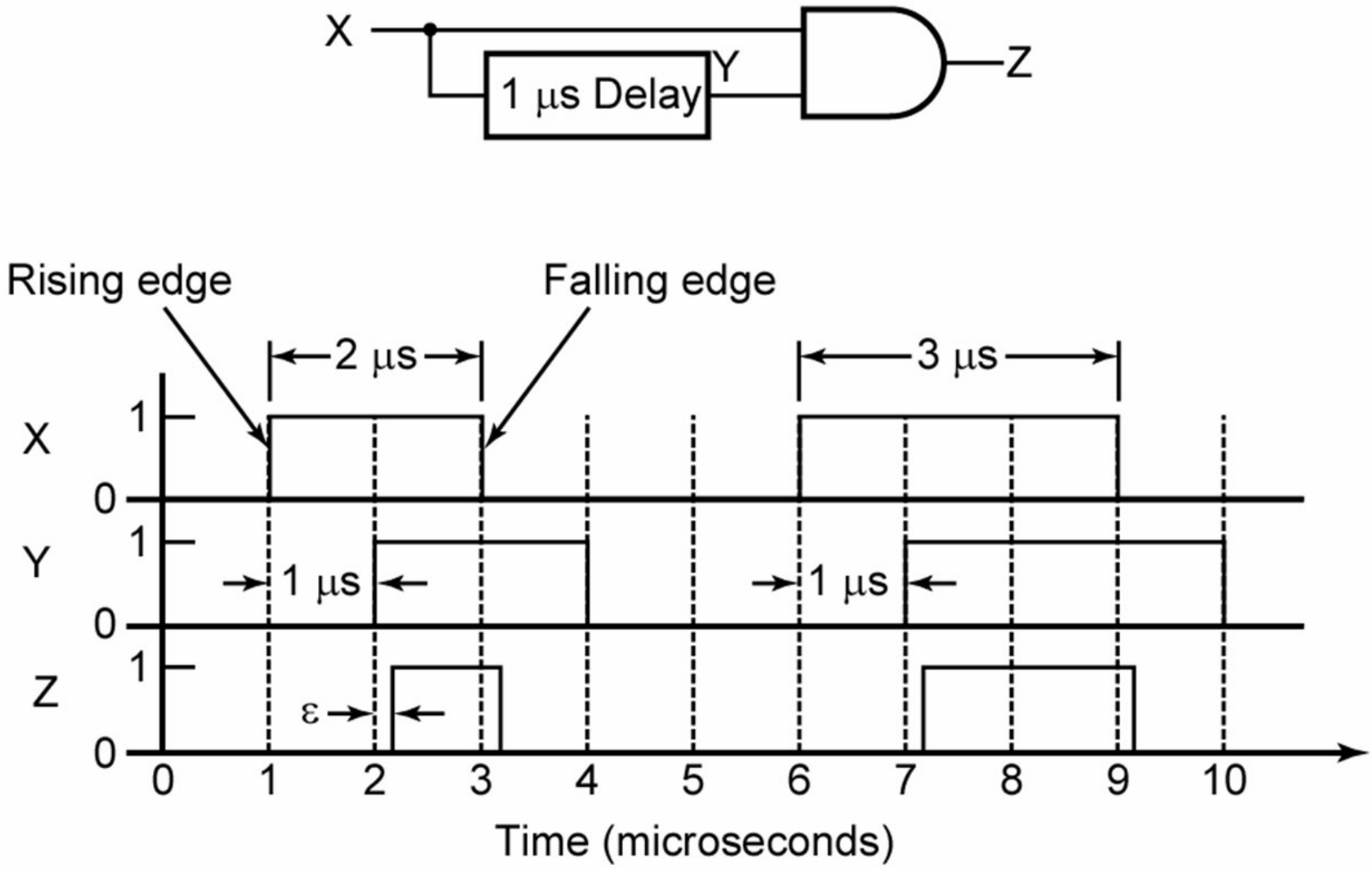


Figure 8-6: **Timing Diagram for Circuit with Delay**

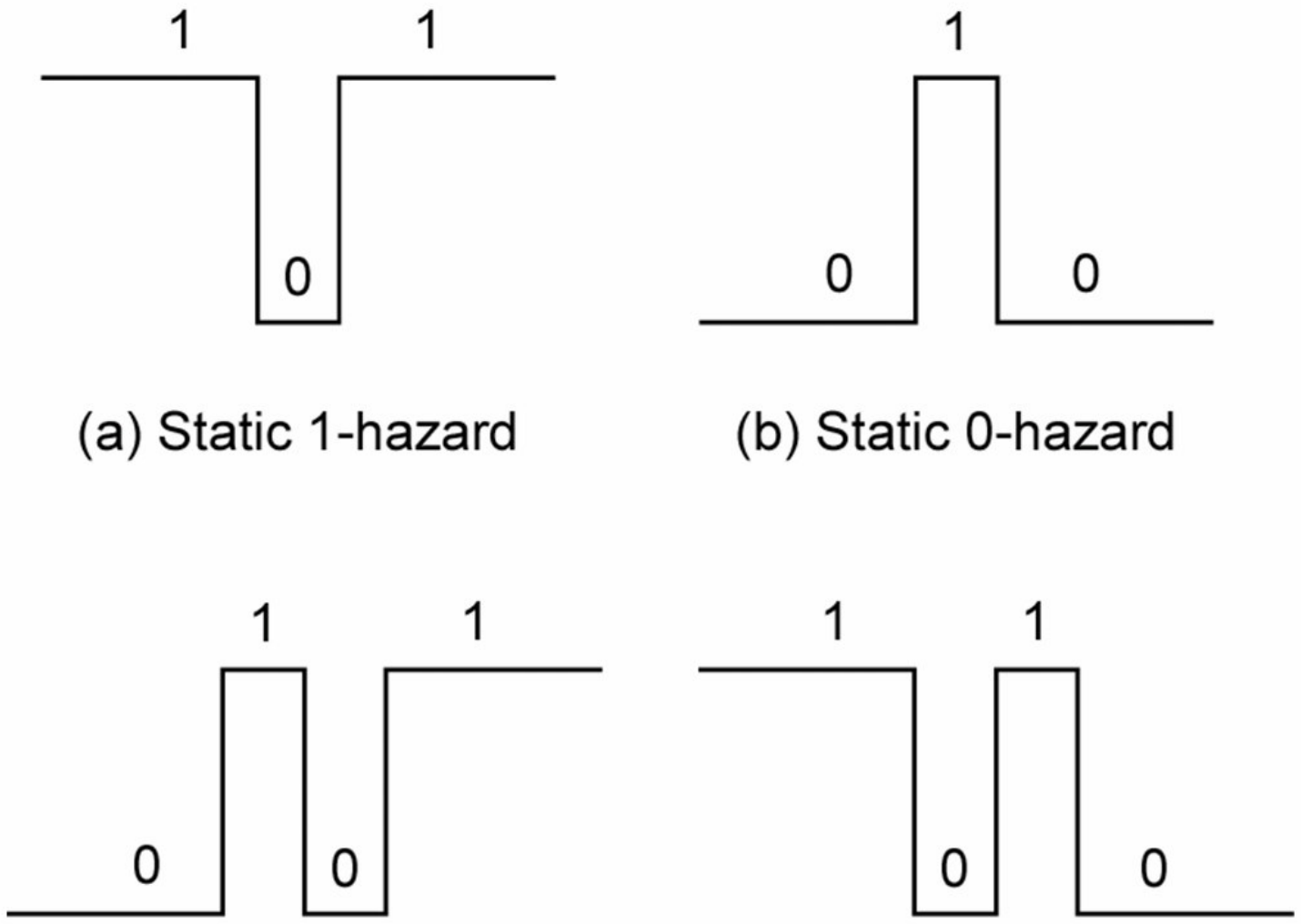
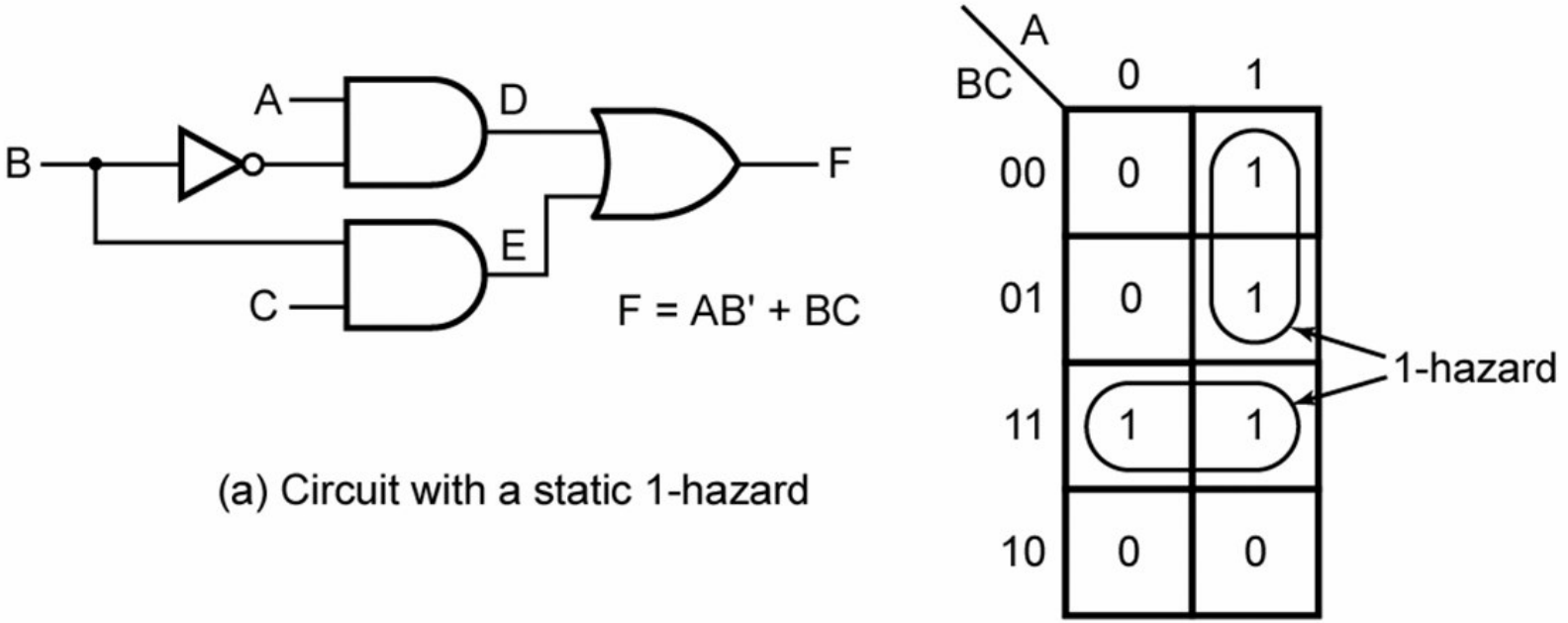
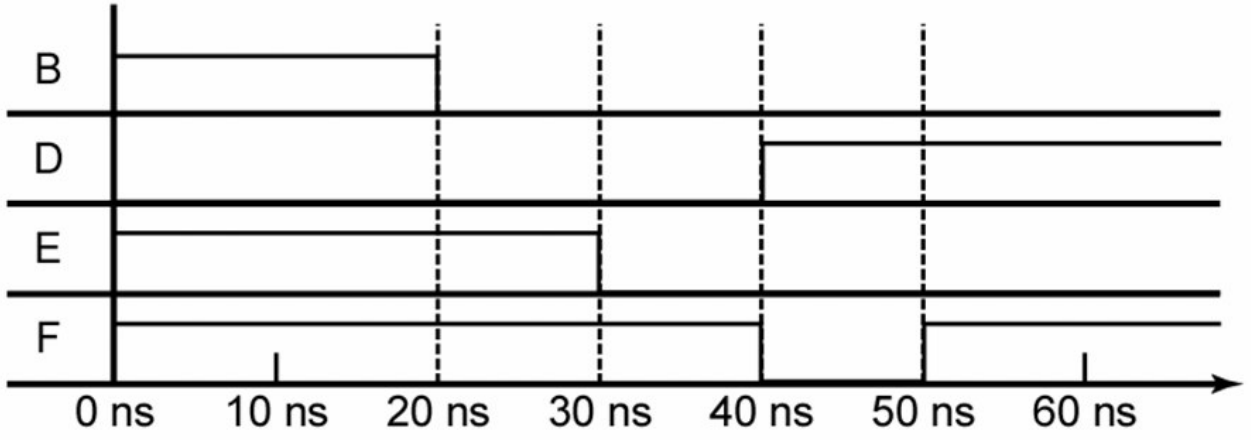


Figure 8-7: **Types of Hazards**



(a) Circuit with a static 1-hazard



(b) Timing chart

Figure 8-8: **Detection of a 1-Hazard**

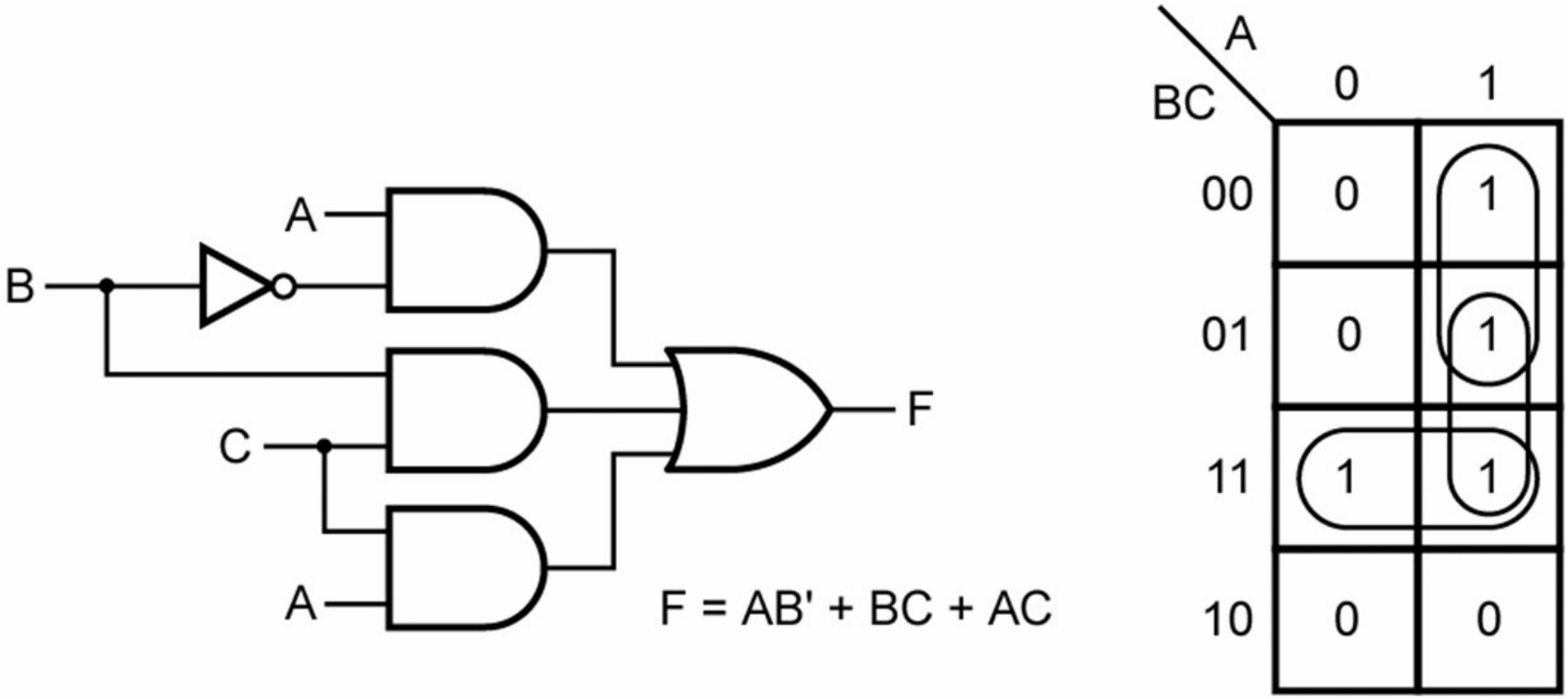
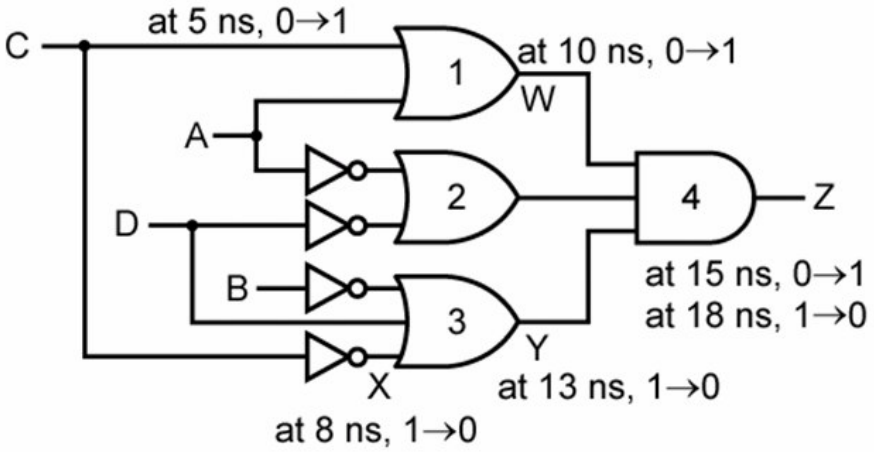
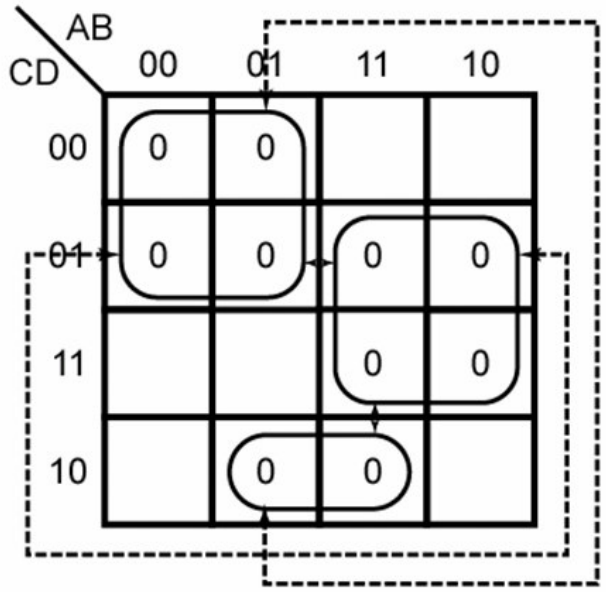


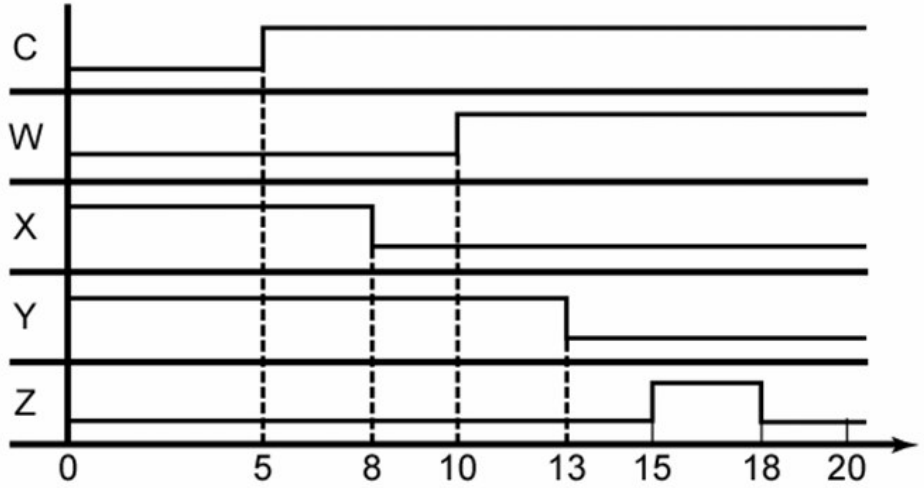
Figure 8-9: **Circuit with Hazard Removed**



(a) Circuit with a static 0-hazard



(b) Karnaugh map for circuit of (a)



(c) Timing diagram illustrating 0-hazard of (a)

Figure 8-10: **Detection of a Static 0-Hazard**

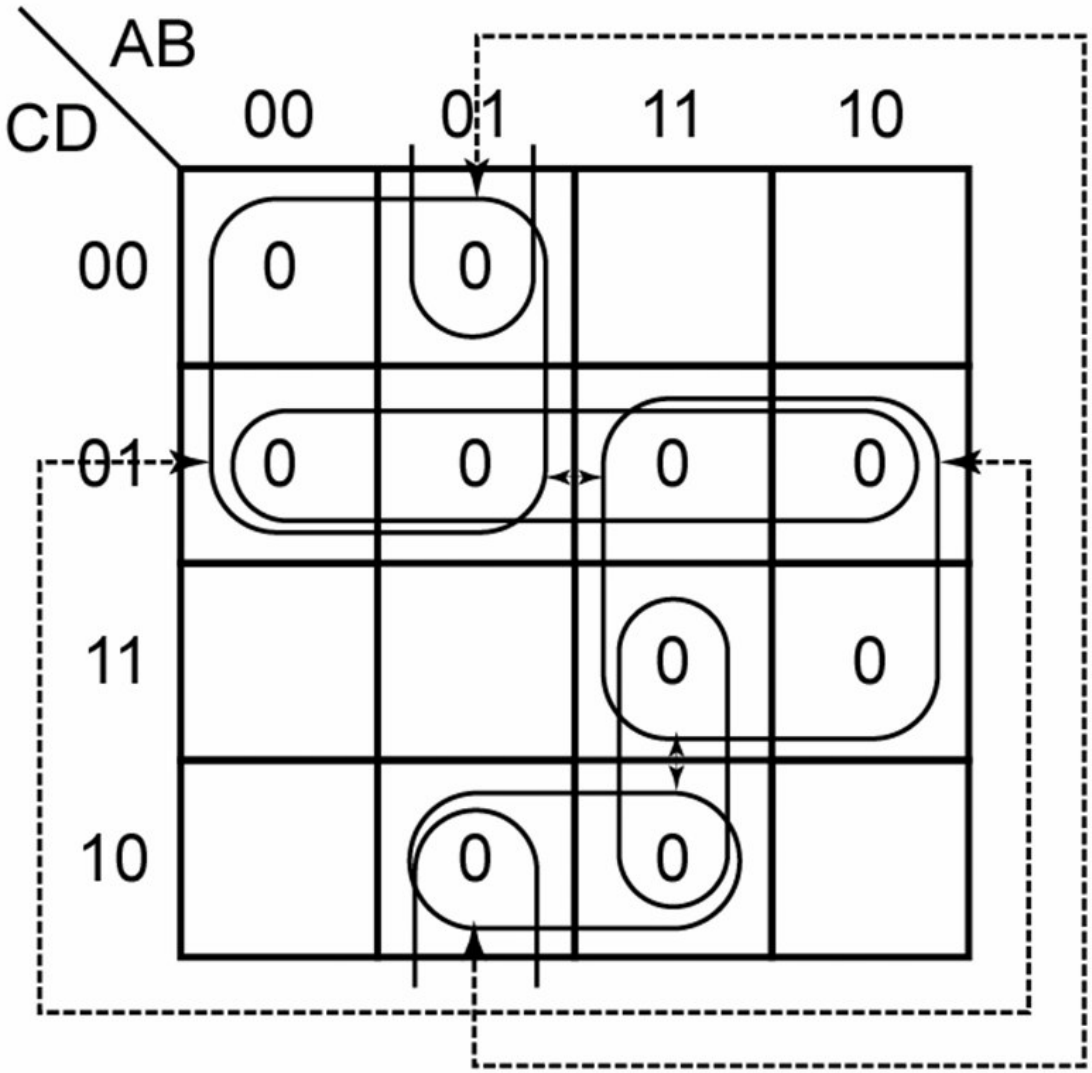
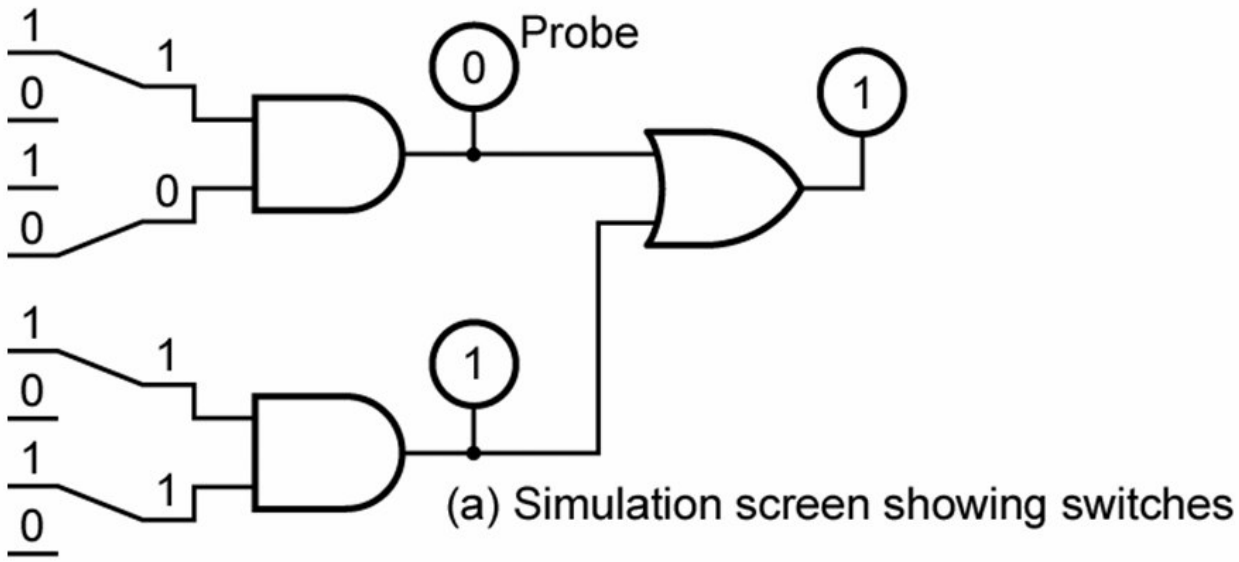


Figure 8-11: **Karnaugh Map Removing Hazards of Figure 8-10**



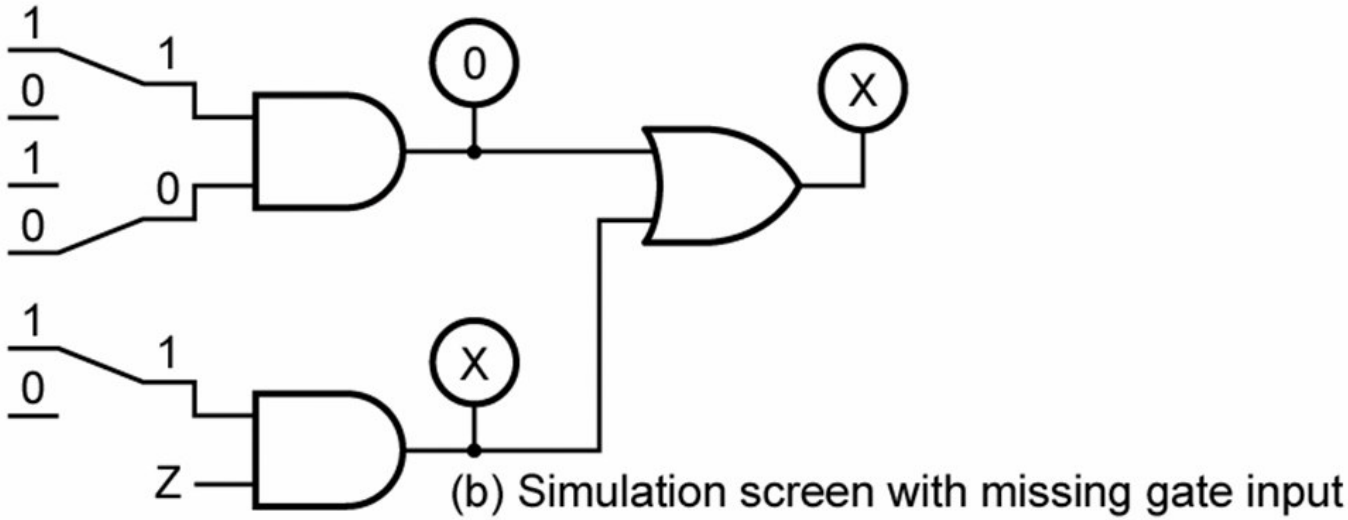


Figure 8-12

•	0	1	X	Z
0	0	0	0	0
1	0	1	X	X
X	0	X	X	X
Z	0	X	X	X

+	0	1	X	Z
0	0	1	X	X
1	1	1	1	1
X	X	1	X	X
Z	X	1	X	X

Table 8-1.
AND and OR Functions for Four-Valued Simulation

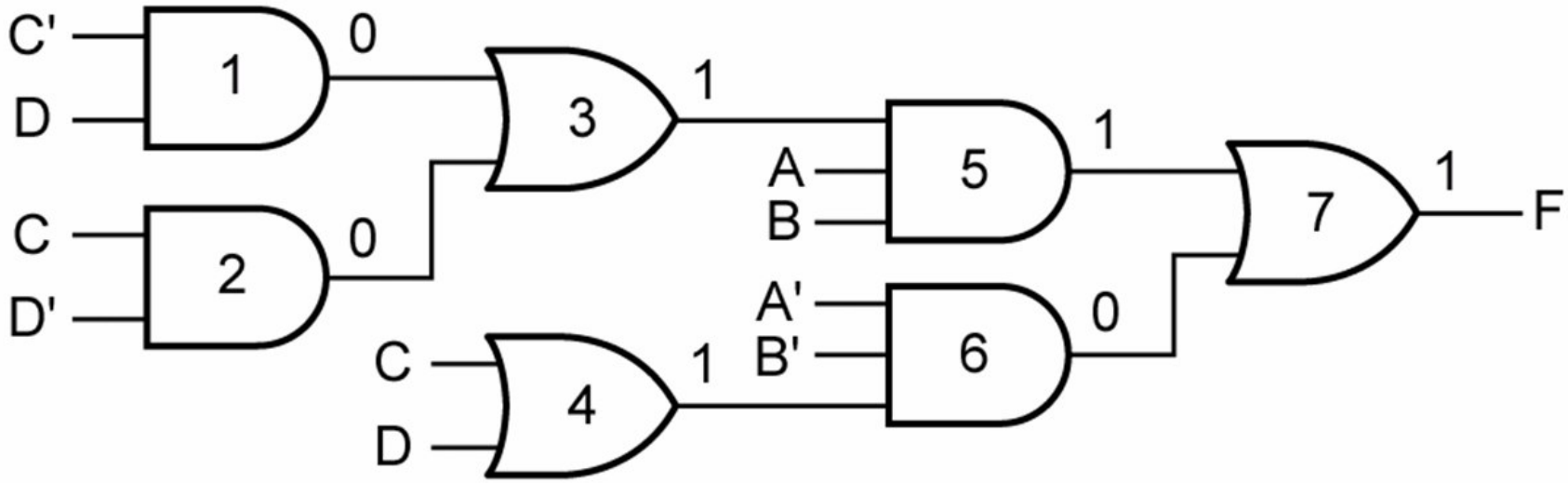


Figure 8-13: **Logic Circuit with Incorrect Output**

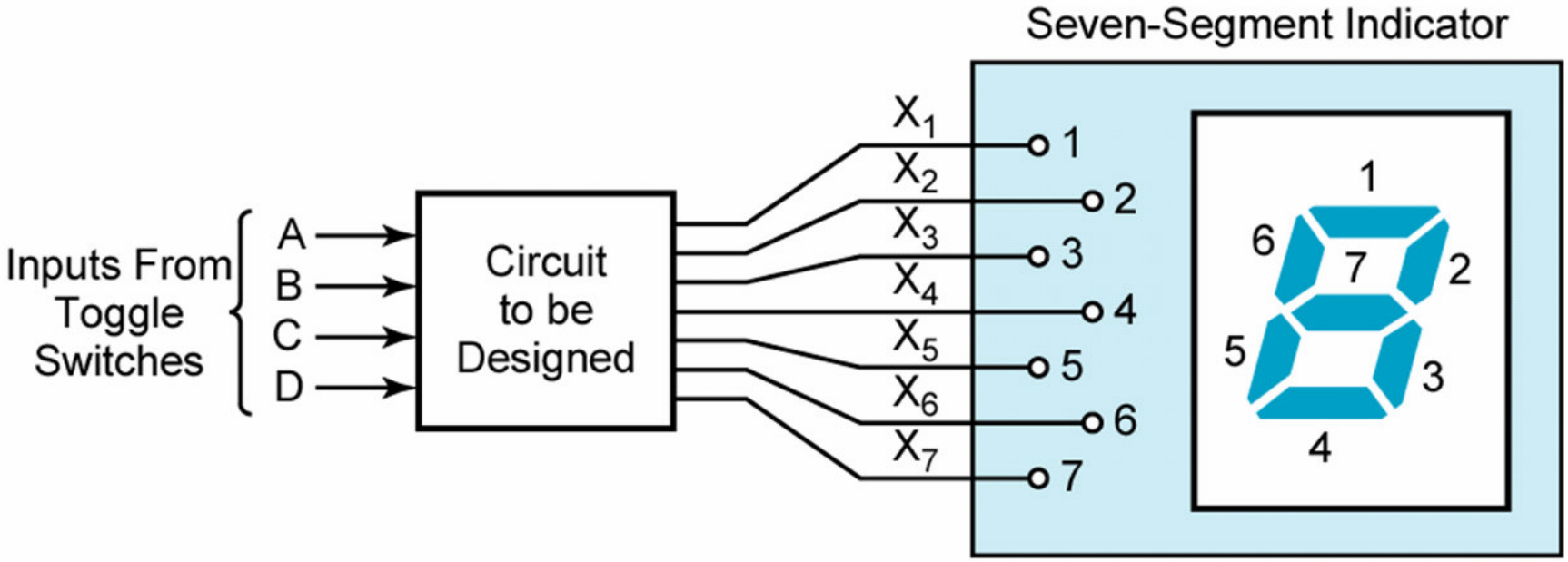


Figure 8.14: **Circuit Driving Seven-Segment Module**