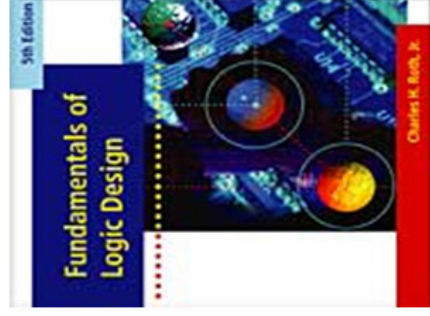


# FIGURES FOR CHAPTER 8

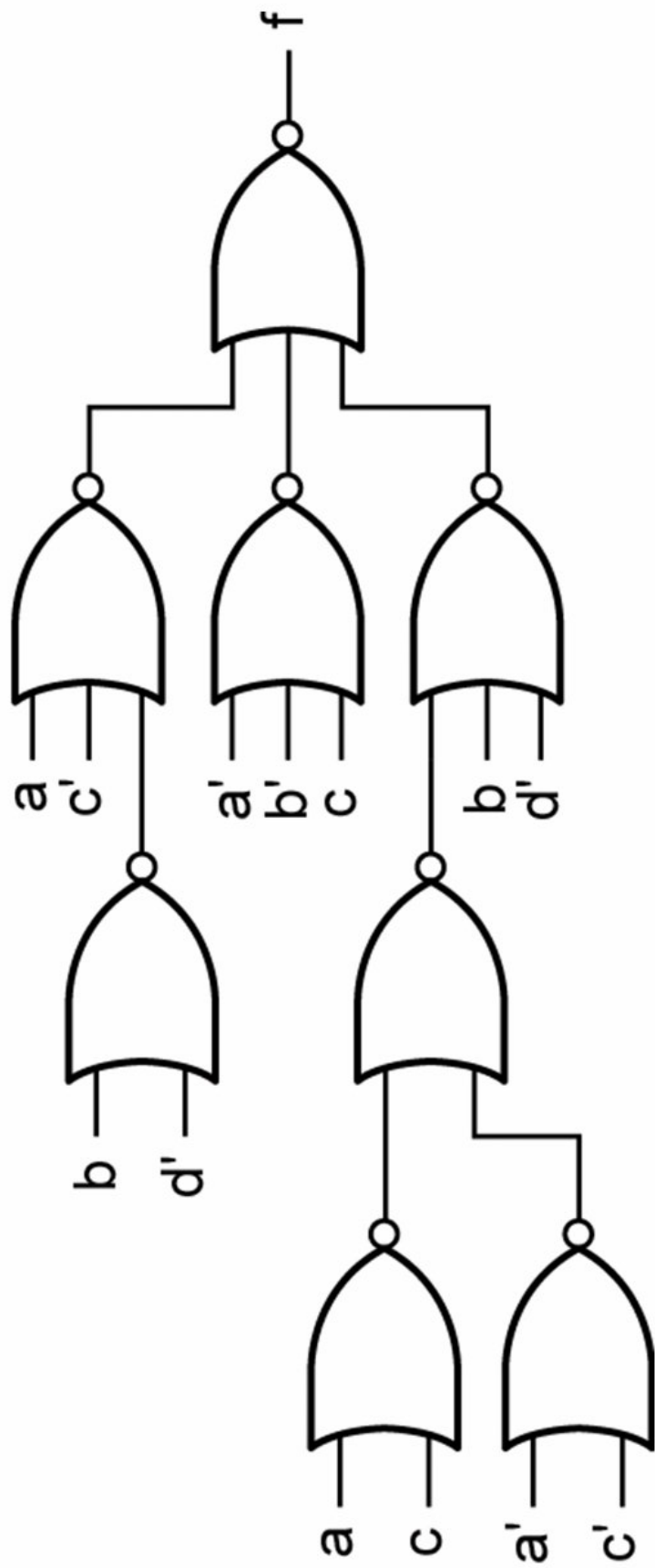
## COMBINATIONAL CIRCUIT DESIGN AND SIMULATION USING GATES



***This chapter in the book includes:***

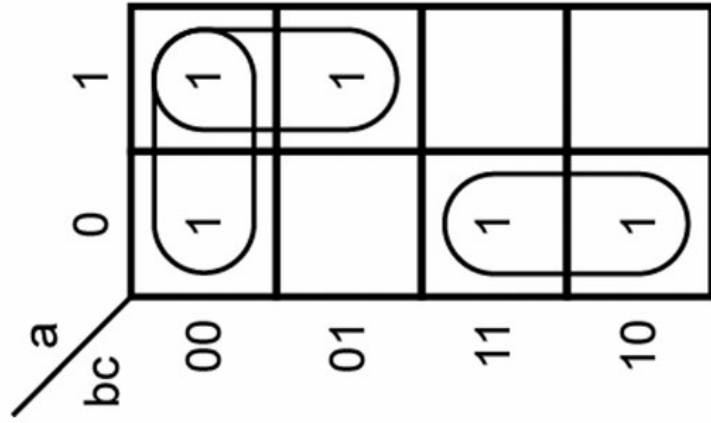
- Objectives
- Study Guide
- 8.1 Review of Combinational Circuit Design
- 8.2 Design Circuits with Limited Gate Fan-In
- 8.3 Gate Delays and Timing Diagrams
- 8.4 Hazards in Combinational Logic
- 8.5 Simulation and Testing of Logic Circuits
- Problems
- Design Problems

**Click the mouse to move to the next page.  
Use the ESC key to exit this chapter.**

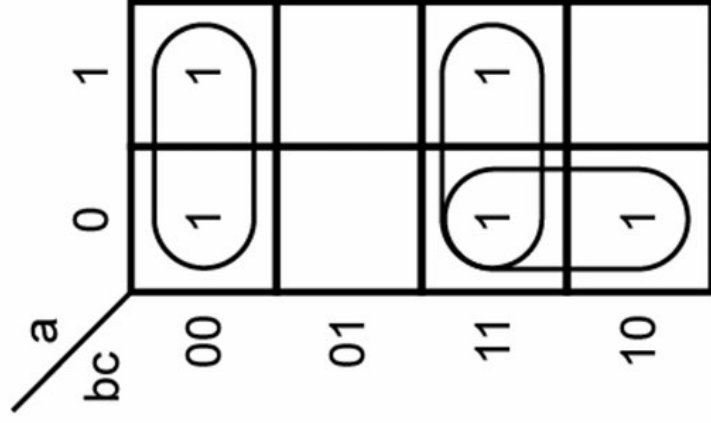


**Figure 8-1**

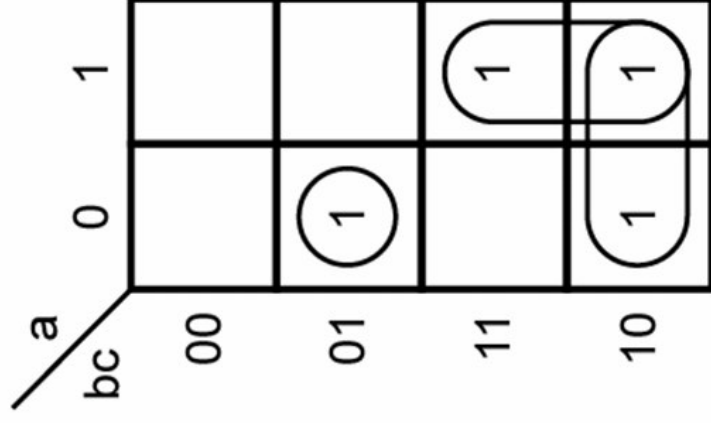




$$f_1 = \Sigma m(0, 2, 3, 4, 5)$$



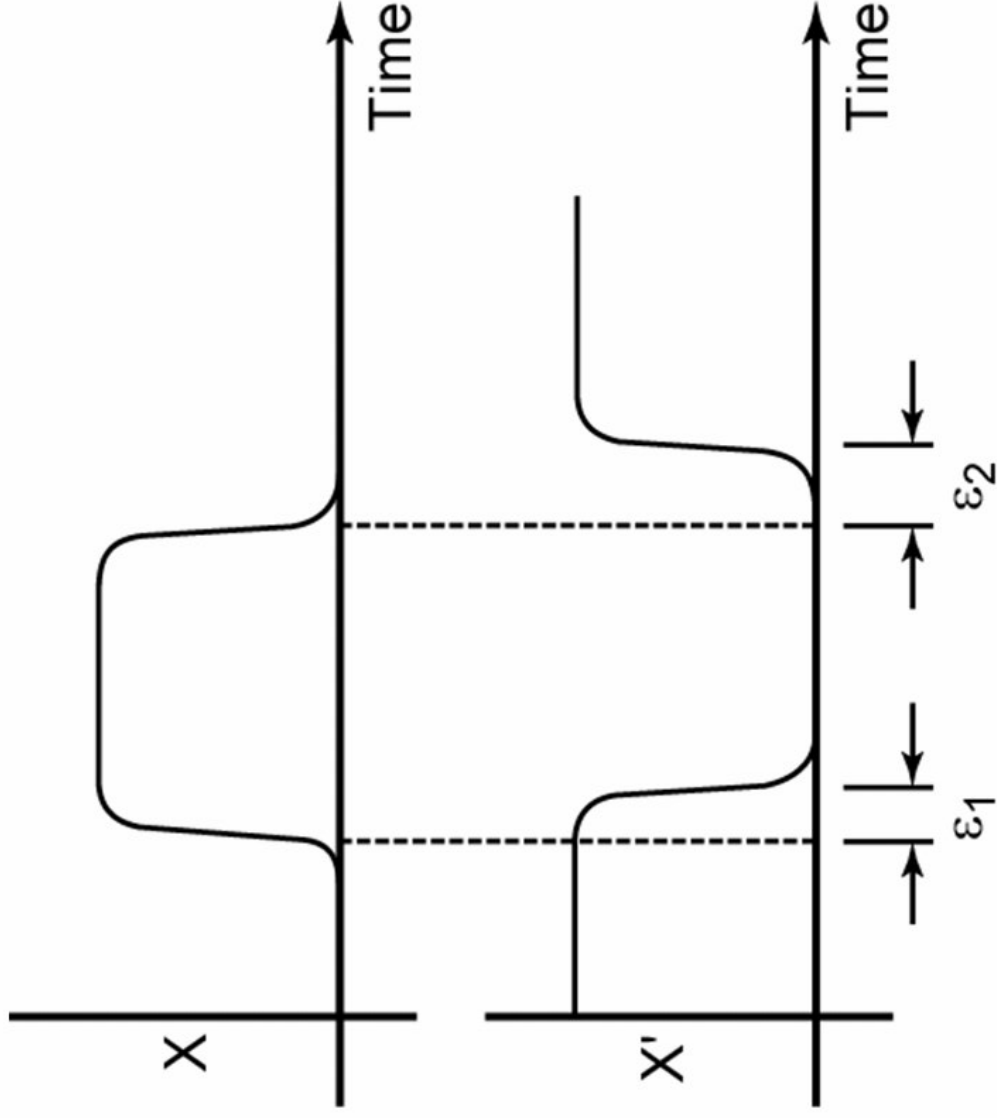
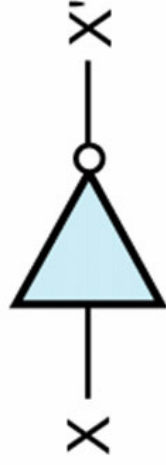
$$f_2 = \Sigma m(0, 2, 3, 4, 7)$$



$$f_3 = \Sigma m(1, 2, 6, 7)$$

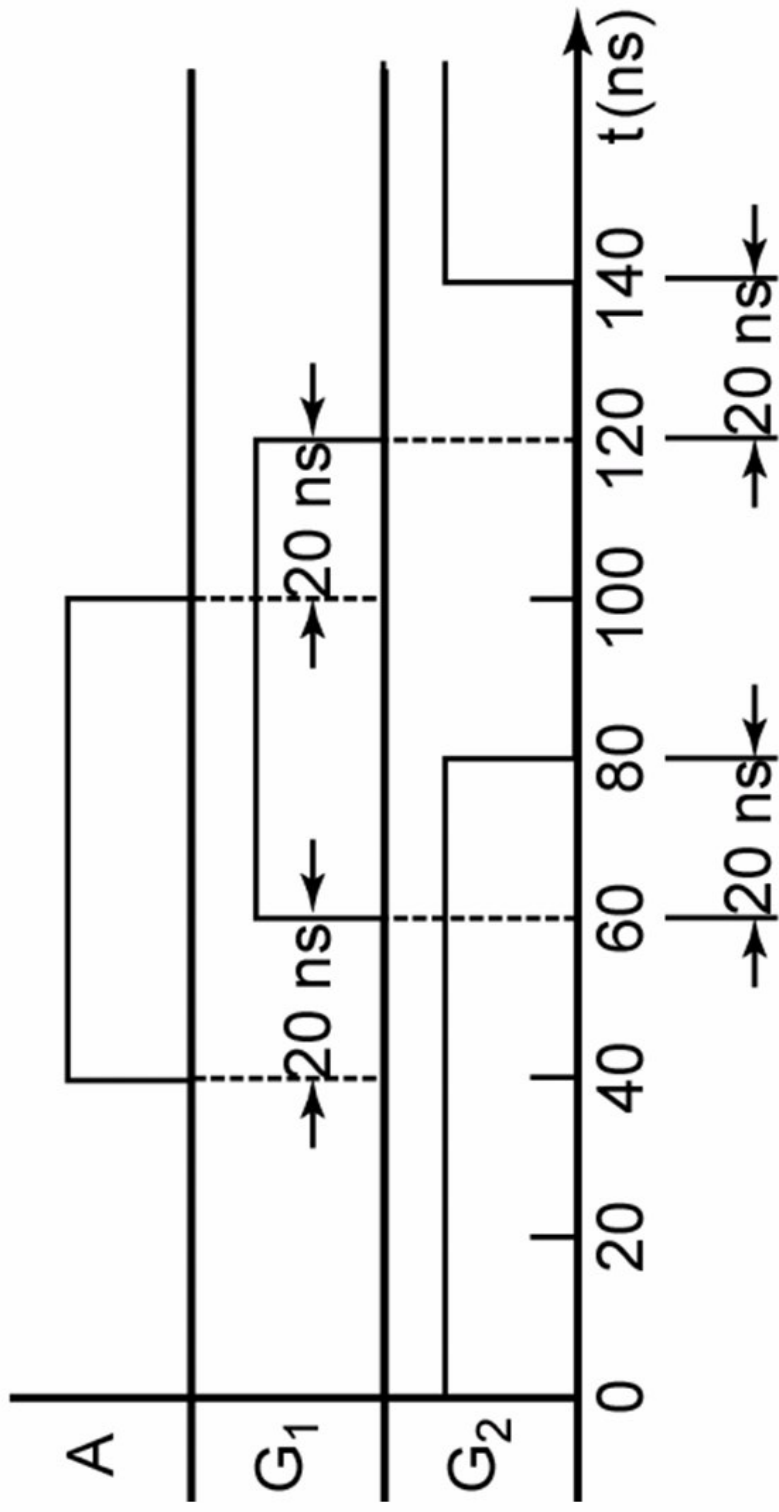
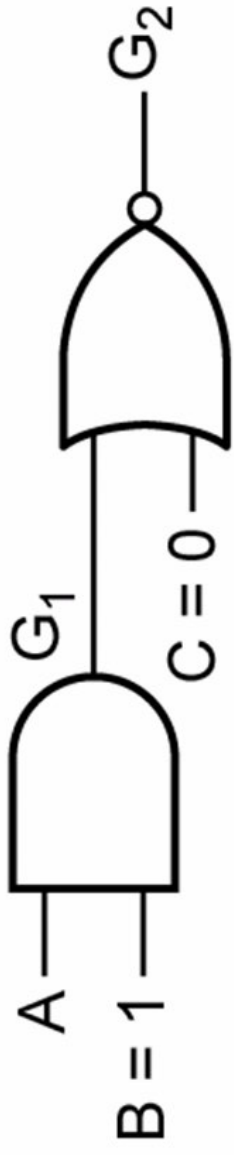
**Figure 8-2**





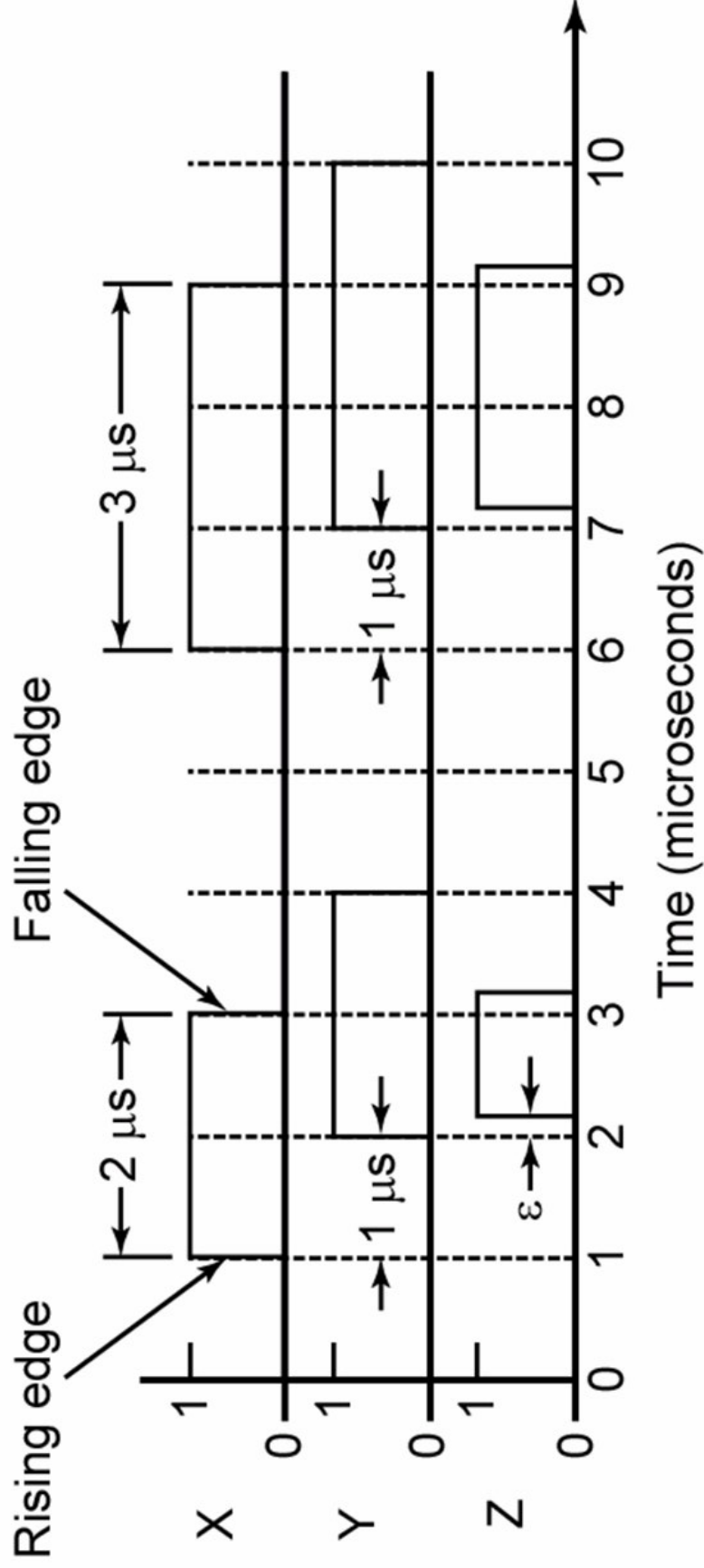
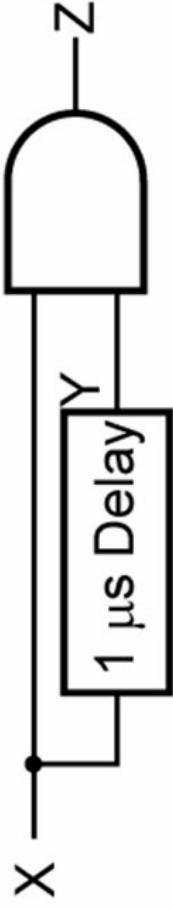
**Figure 8-4: Propagation Delay in an Inverter**



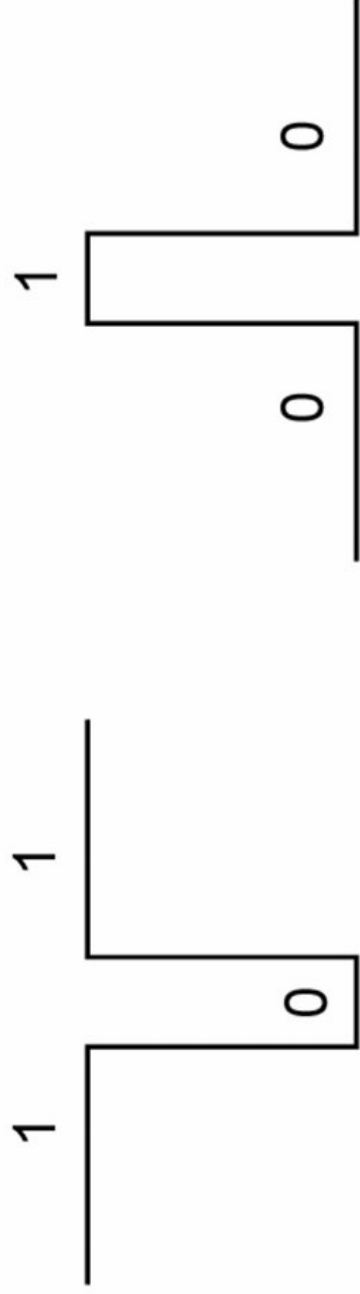


**Figure 8-5: Timing Diagram for AND-NOR Circuit**

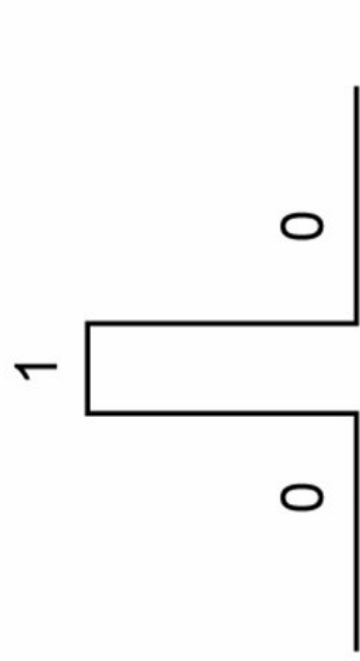




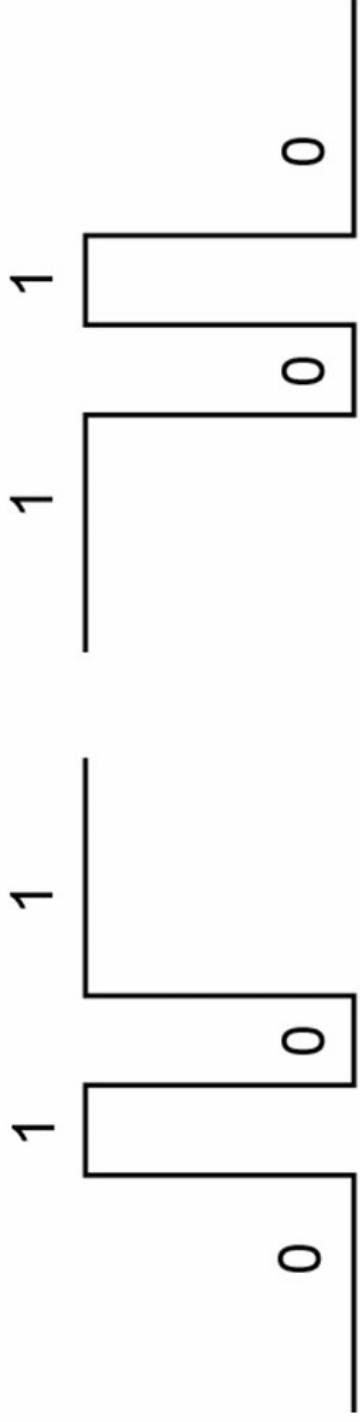
**Figure 8-6: Timing Diagram for Circuit with Delay**



(a) Static 1-hazard



(b) Static 0-hazard

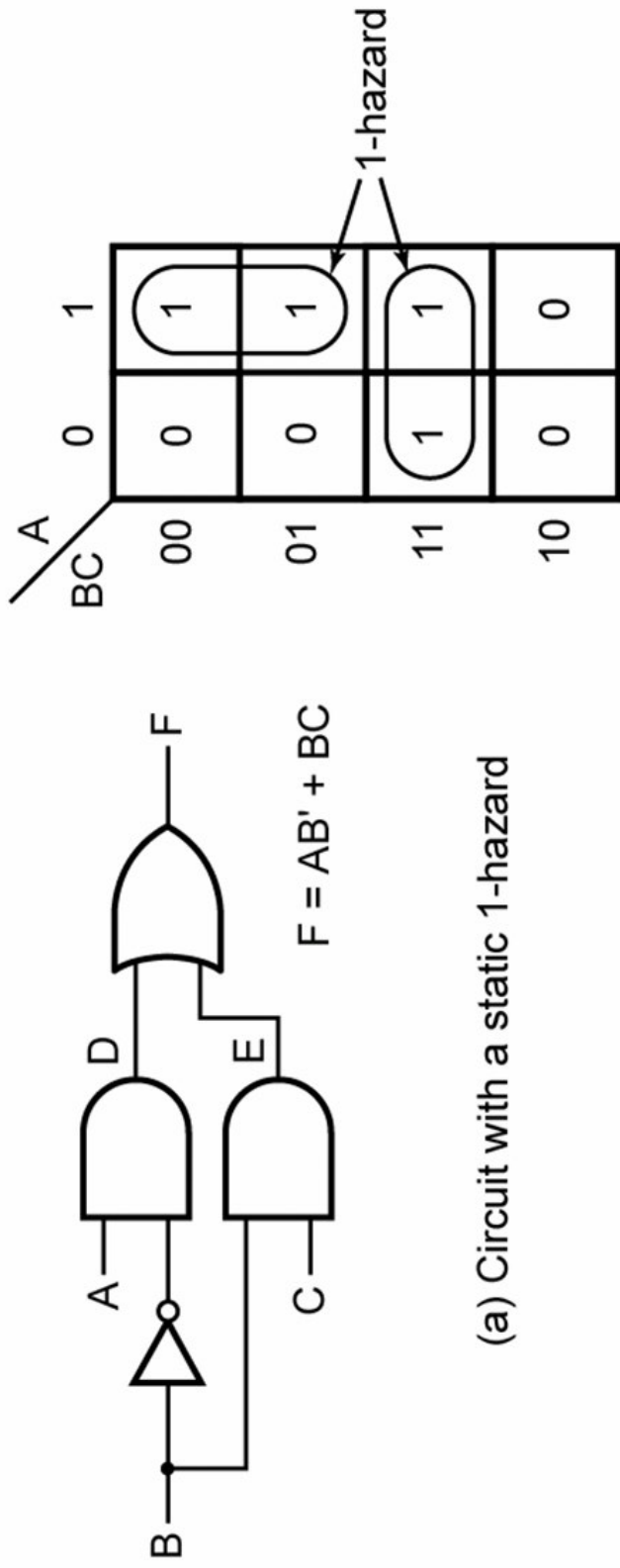


(c) Dynamic hazards

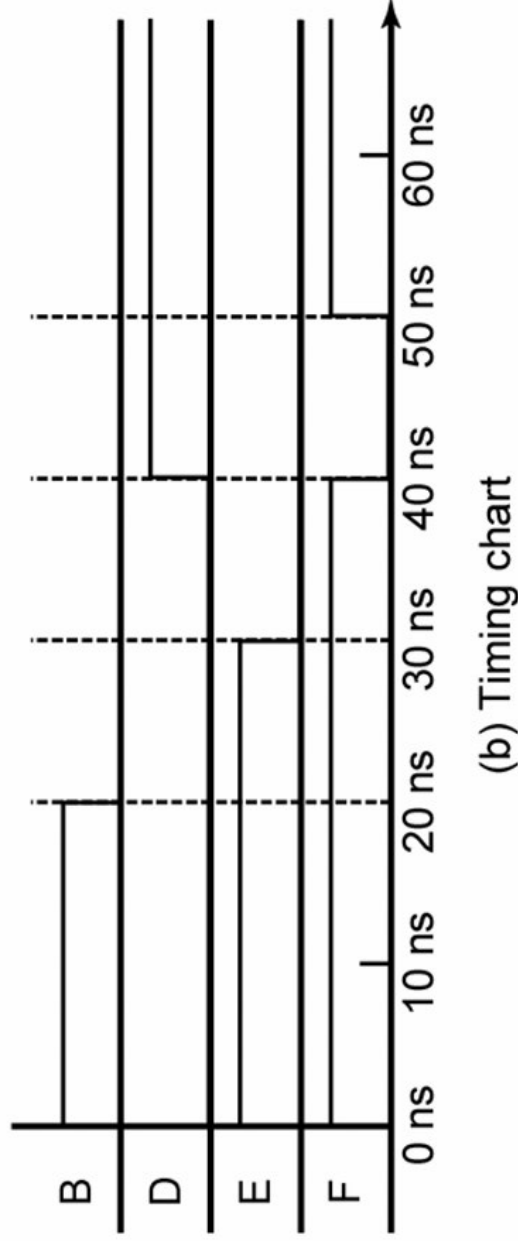
**Figure 8-7: Types of Hazards**





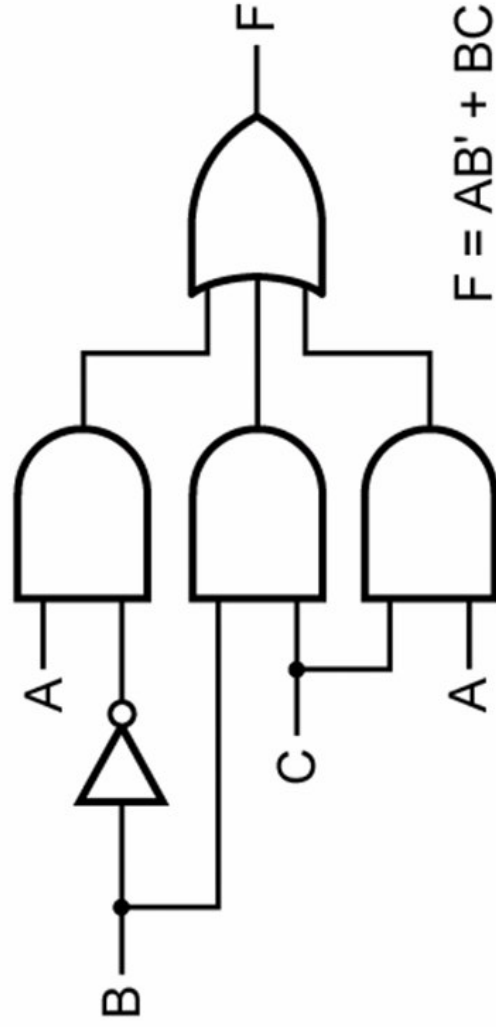


(a) Circuit with a static 1-hazard



**Figure 8-8: Detection of a 1-Hazard**

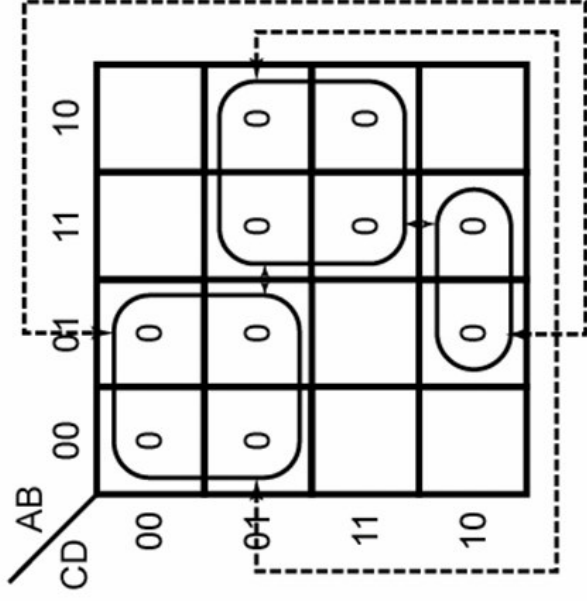




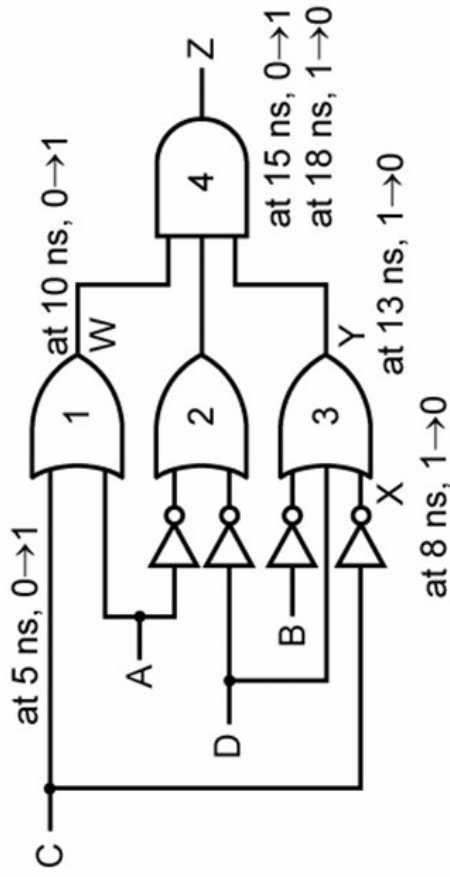
$$F = AB' + BC + AC$$

	A	0	1
BC	00	0	1
	01	0	1
	11	1	1
	10	0	0

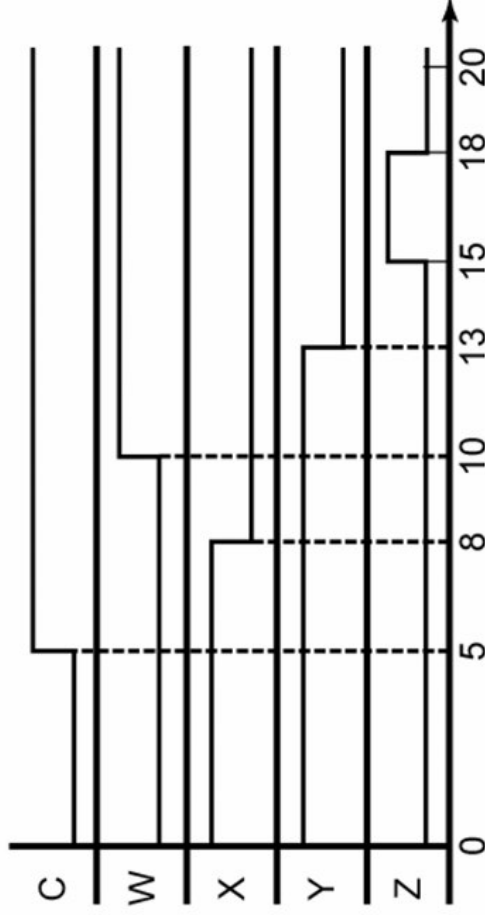
**Figure 8-9: Circuit with Hazard Removed**



(b) Karnaugh map for circuit of (a)



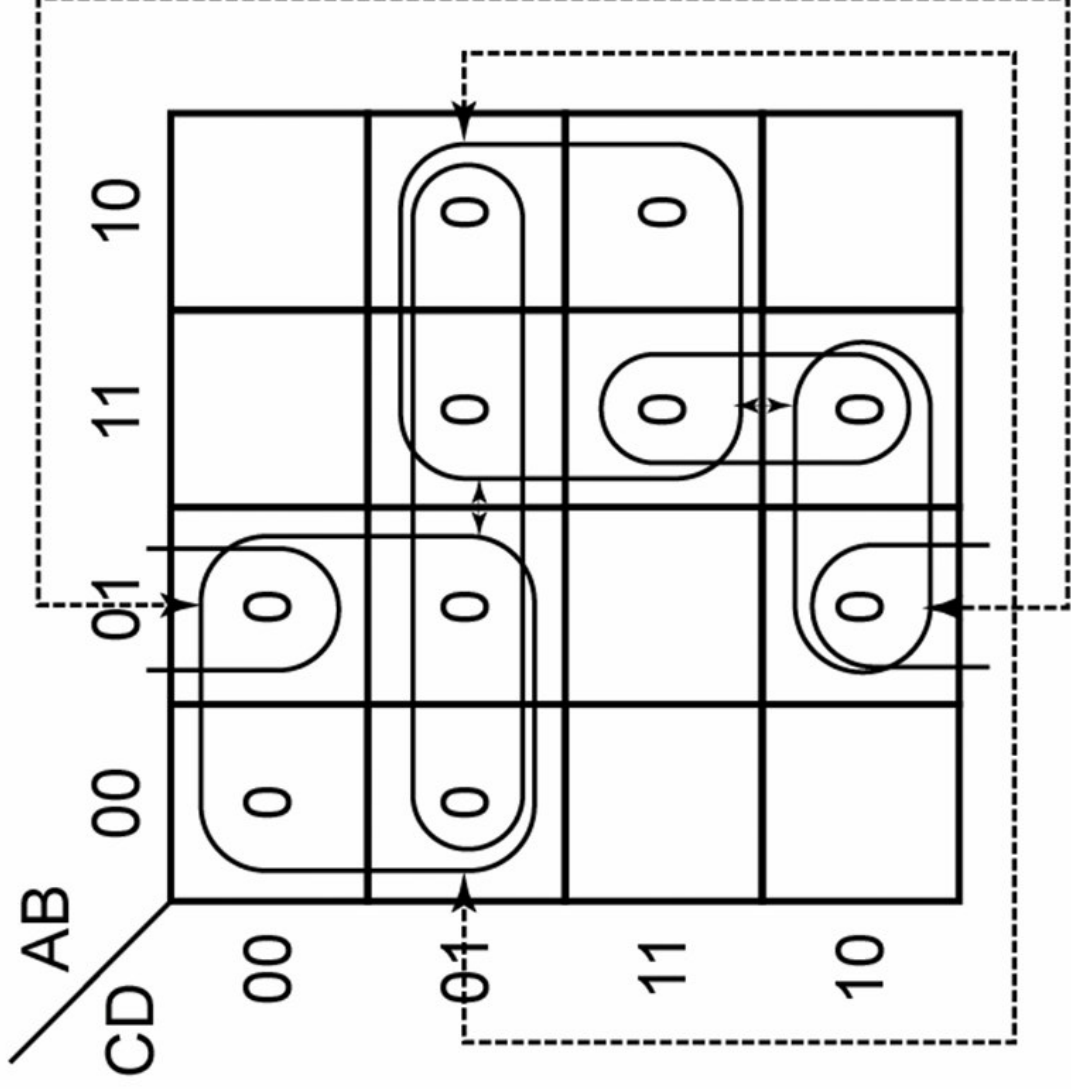
(a) Circuit with a static 0-hazard



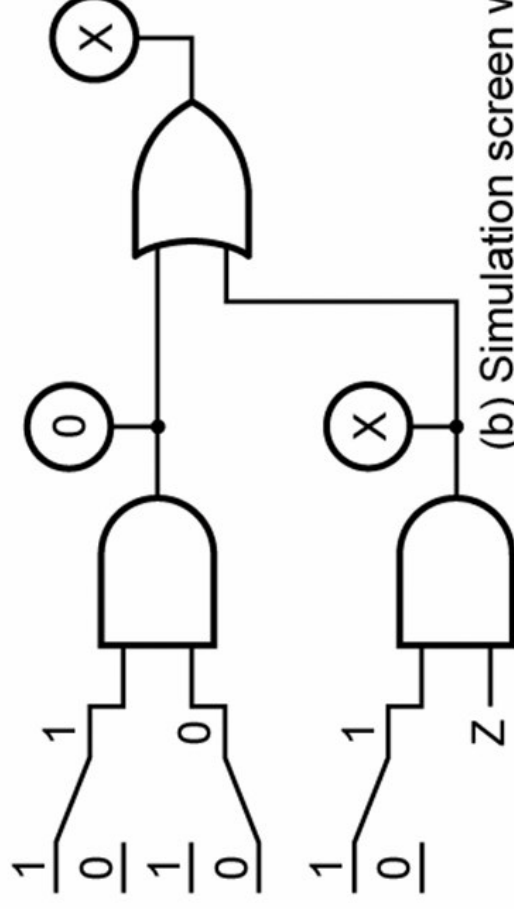
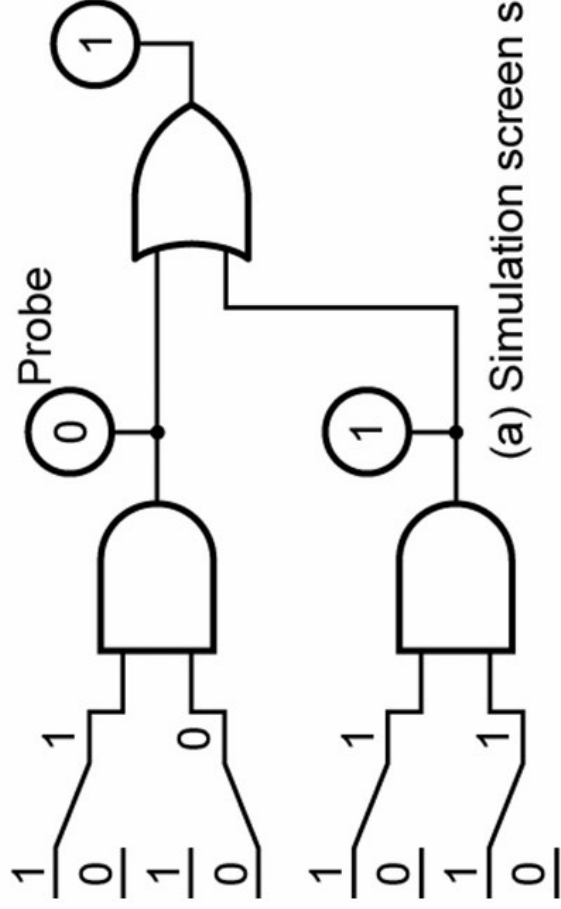
(c) Timing diagram illustrating 0-hazard of (a)

**Figure 8-10: Detection of a Static 0-Hazard**





**Figure 8-11: Karnaugh Map Removing Hazards of Figure 8-10**

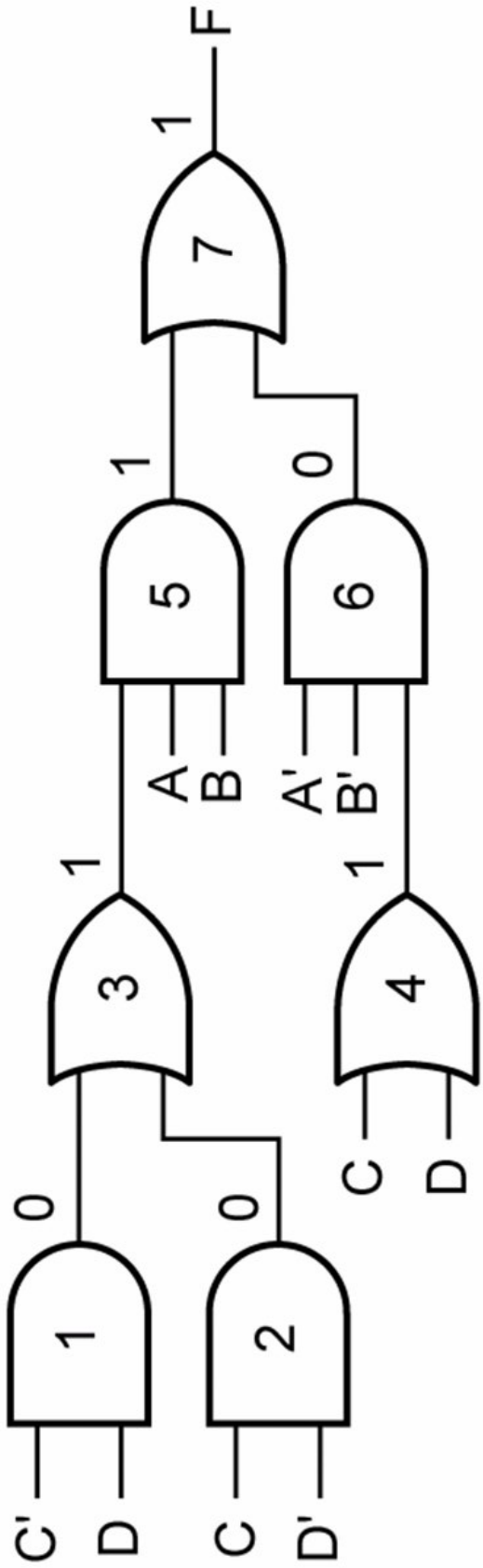


**Figure 8-12**

$\cdot$	0	1	X	Z		+	0	1	X	Z
0	0	0	0	0	0	0	0	1	X	X
1	0	1	X	X	1	1	1	1	1	1
X	0	X	X	X	X	X	X	1	X	X
Z	0	X	X	X	Z	Z	X	1	X	X

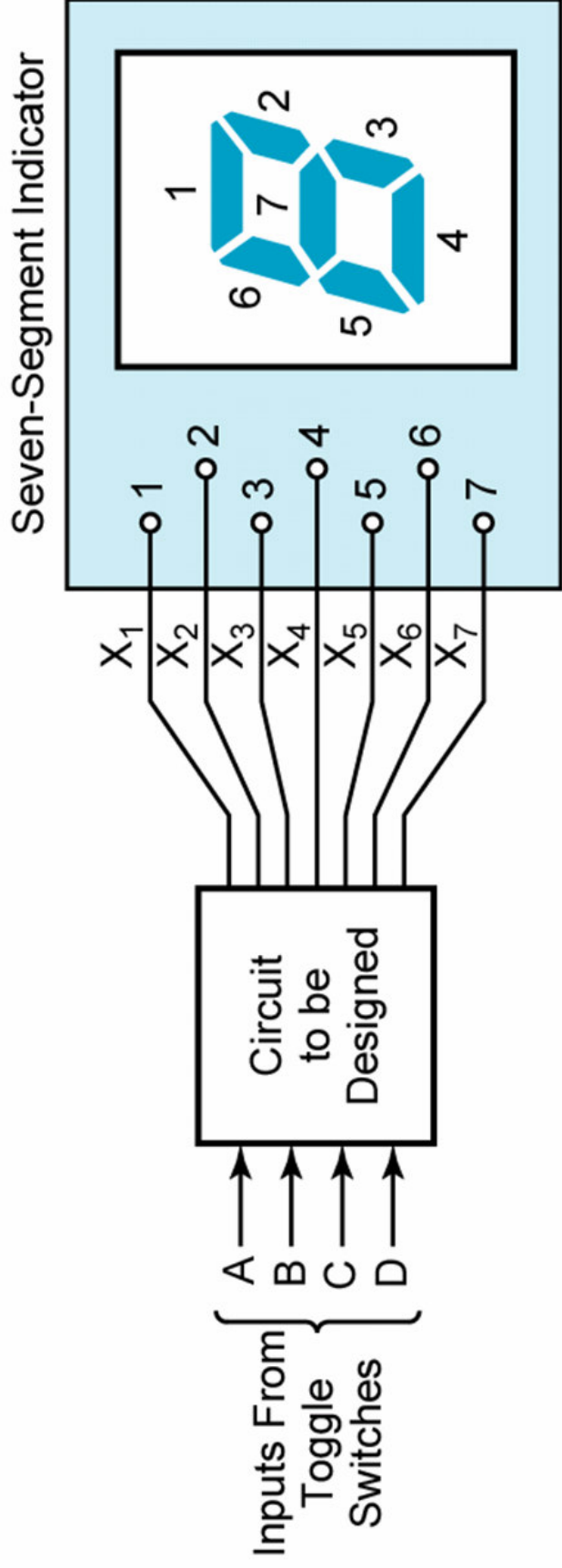
**Table 8-1.**  
**AND and OR Functions for Four-Valued Simulation**





**Figure 8-13: Logic Circuit with Incorrect Output**





**Figure 8.14: Circuit Driving Seven-Segment Module**