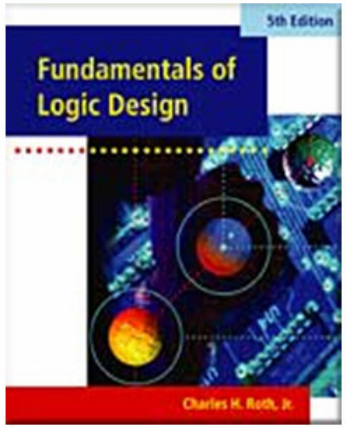
FIGURES FOR

CHAPTER 7

MULTI-LEVEL GATE CIRCUITS
NAND AND NOR GATES



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Use the ESC key to exit this chapter.

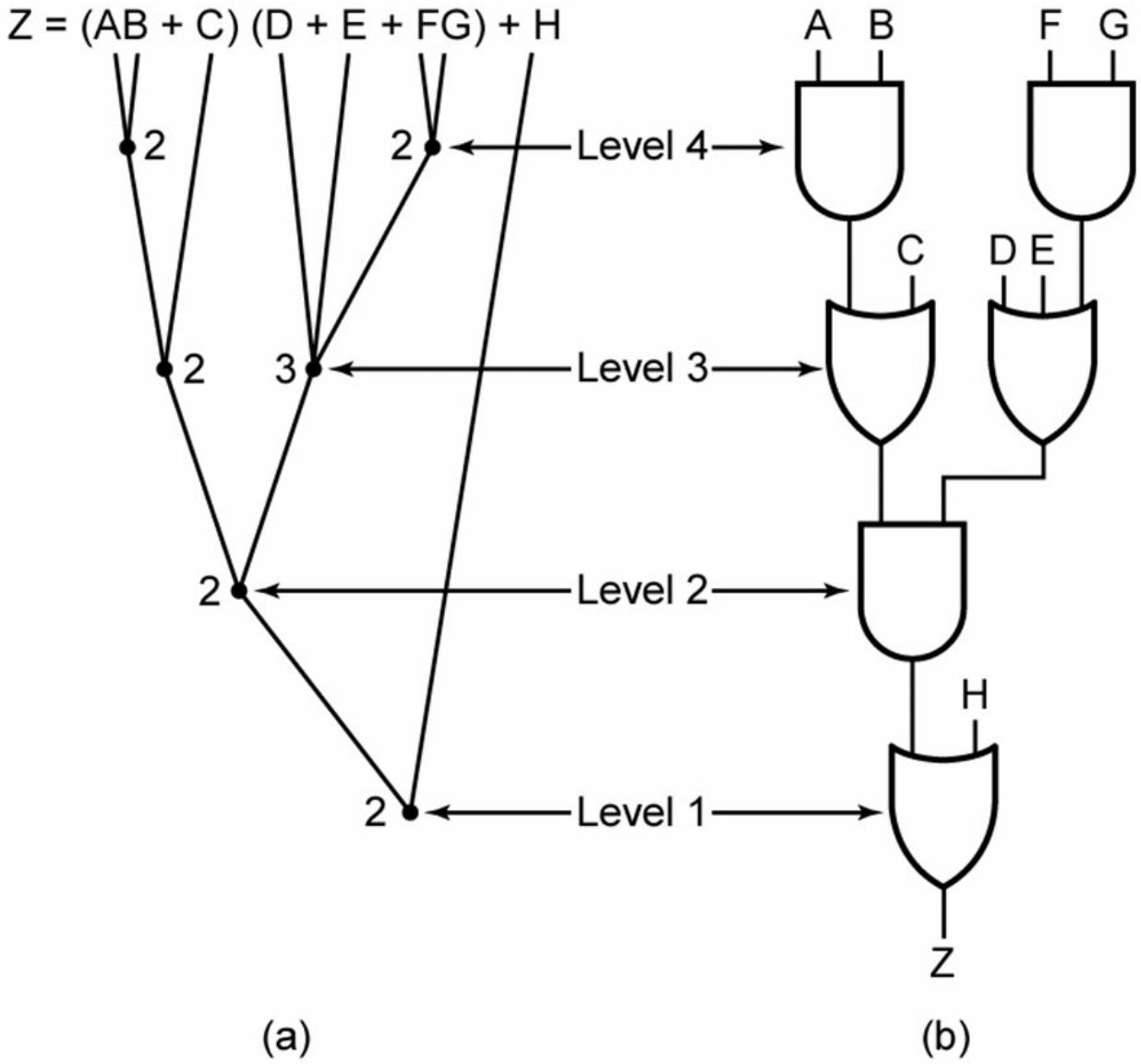


Figure 7-1: **Four-Level Realization of Z**

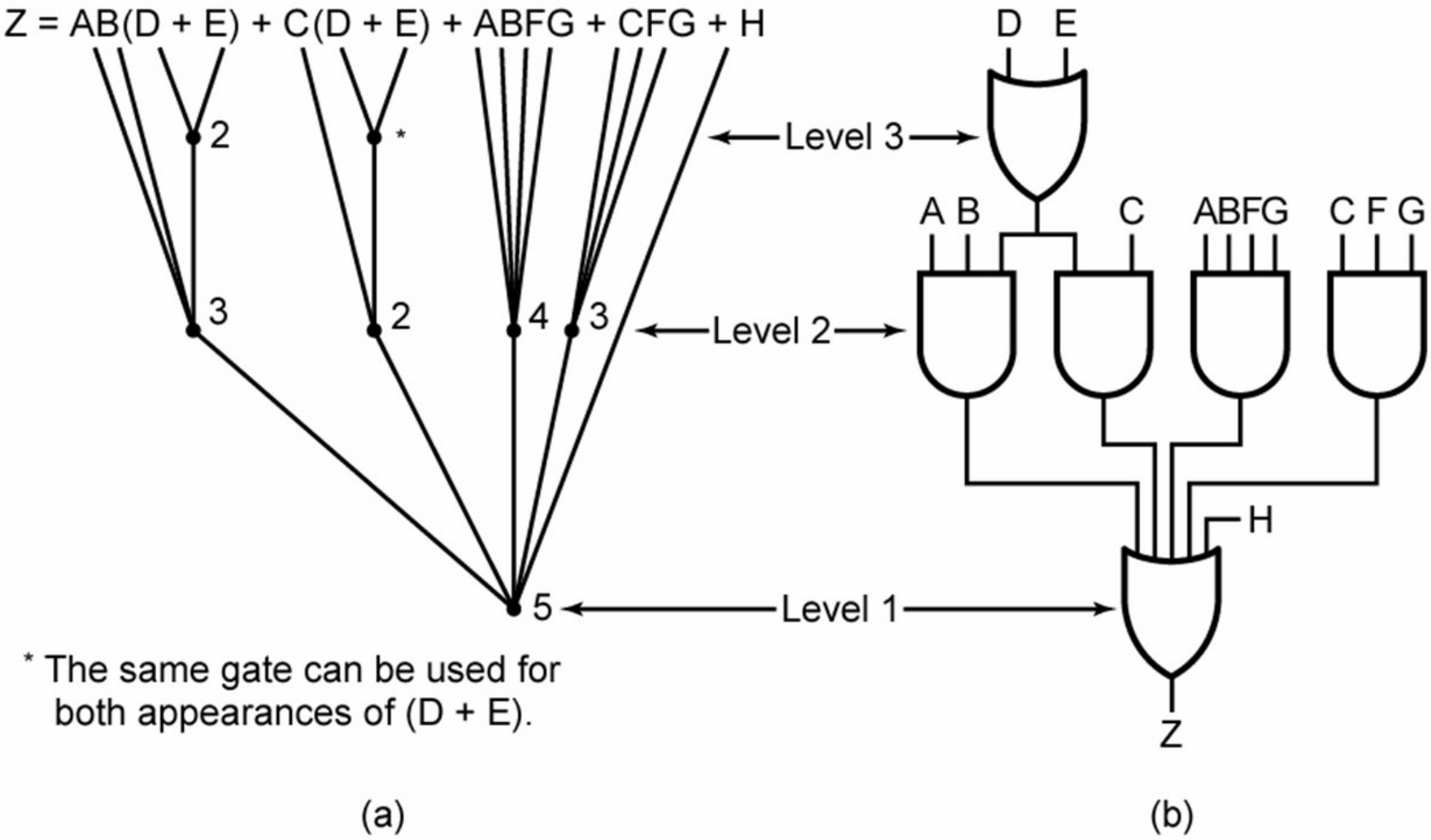
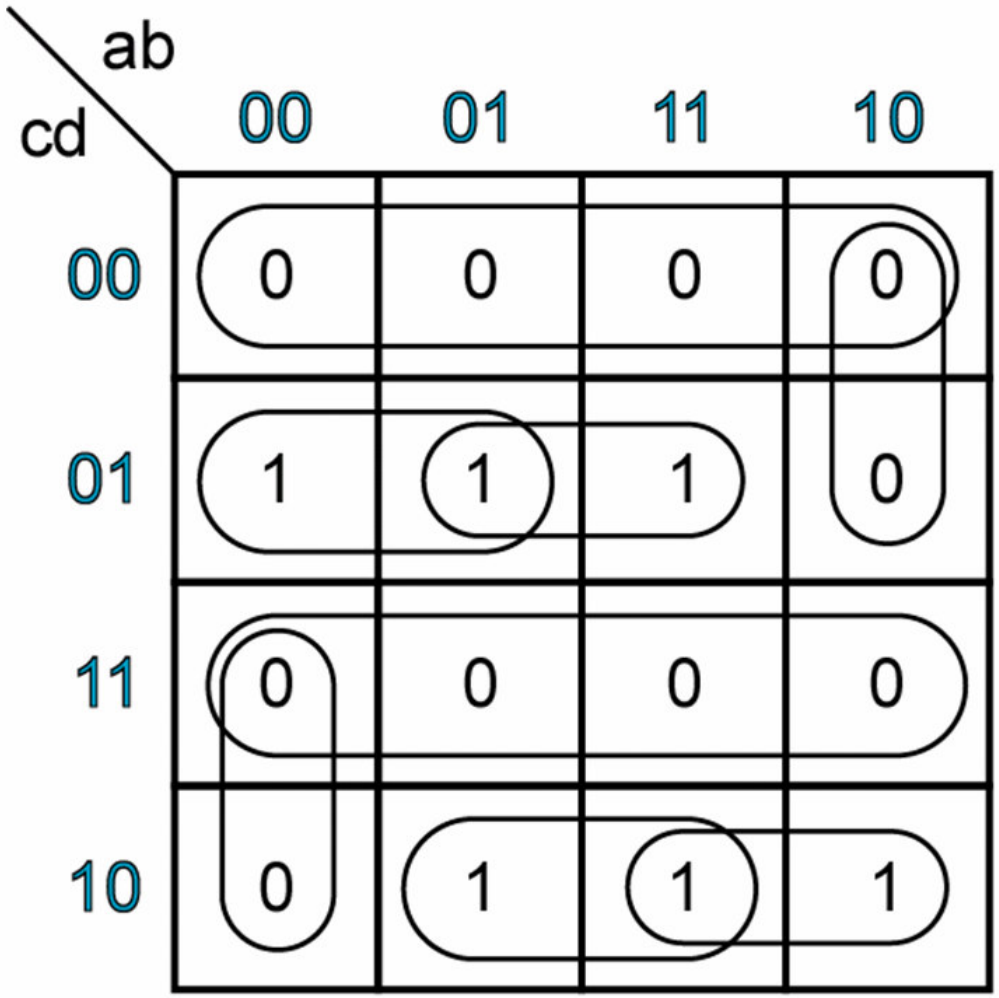


Figure 7-2: **Three-Level Realization of Z**



$f = a'c'd + bc'd + bcd' + acd'$

Figure 7-3

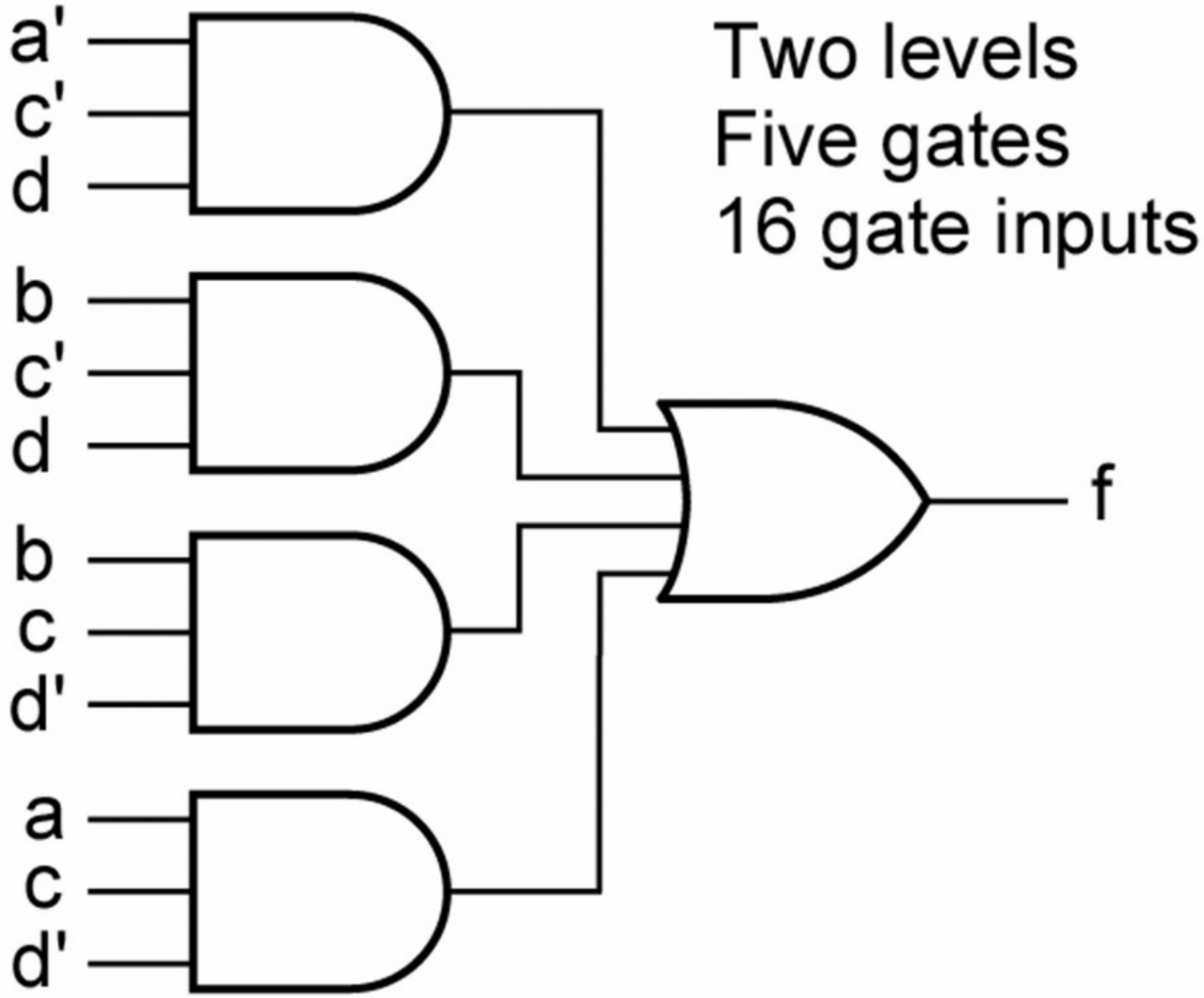


Figure 7-4

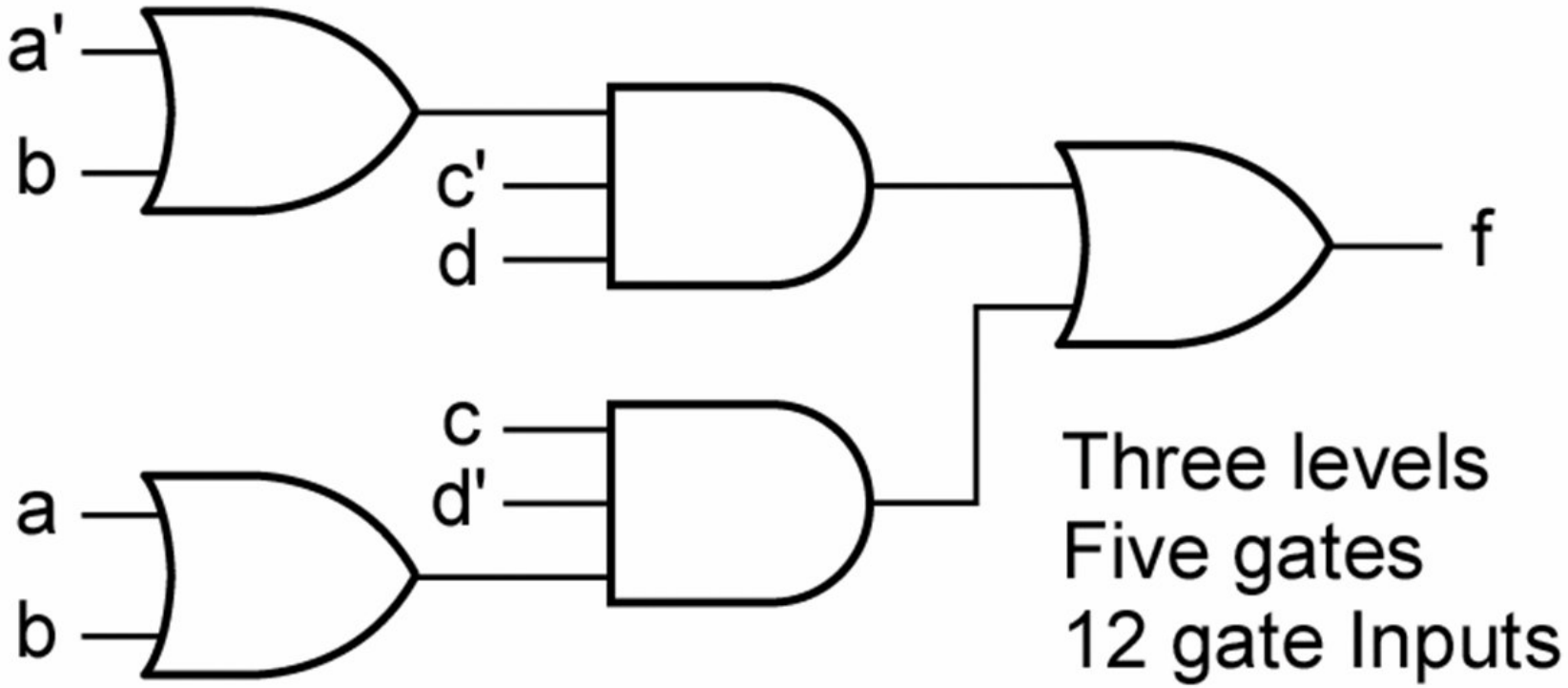


Figure 7-5

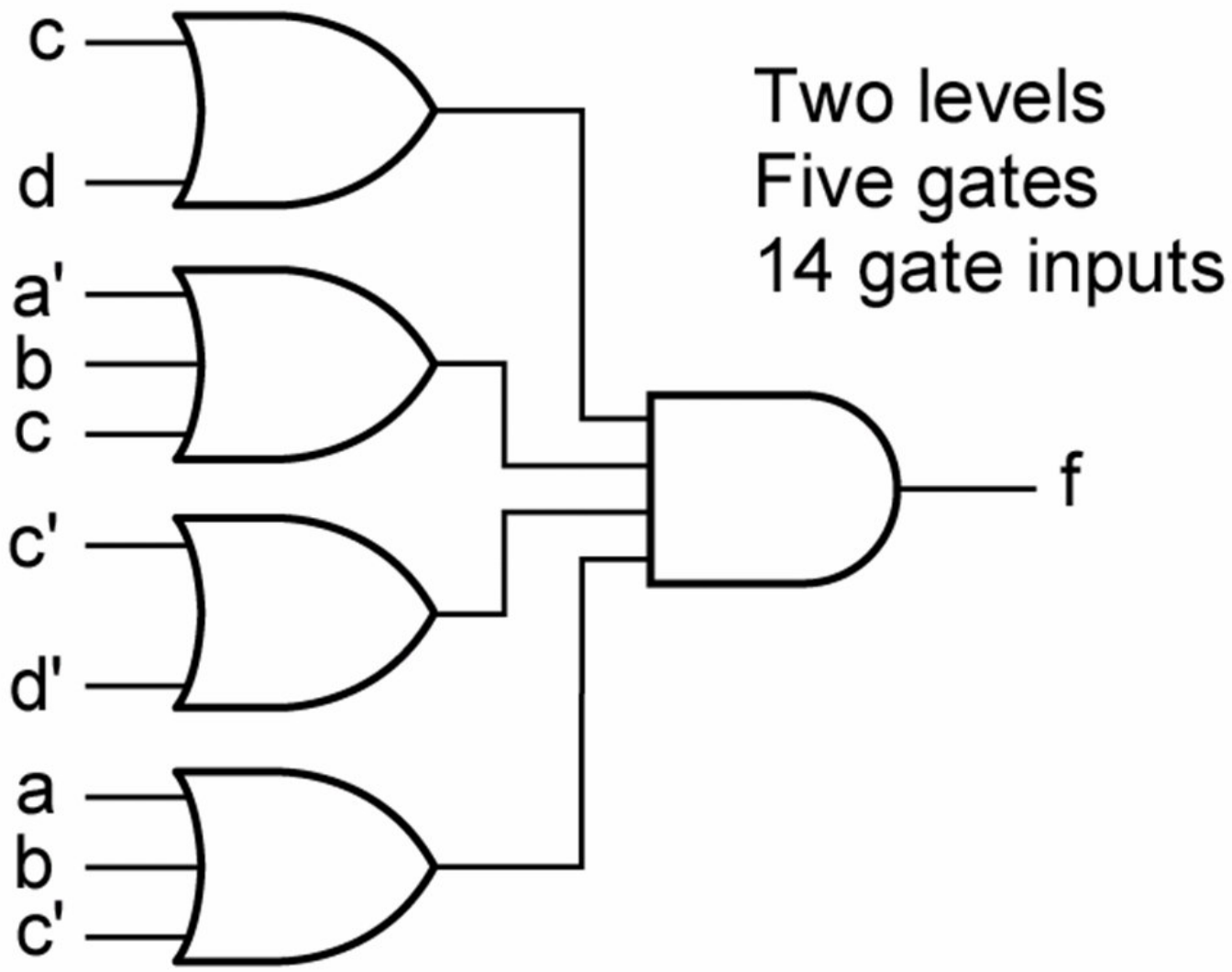


Figure 7-6

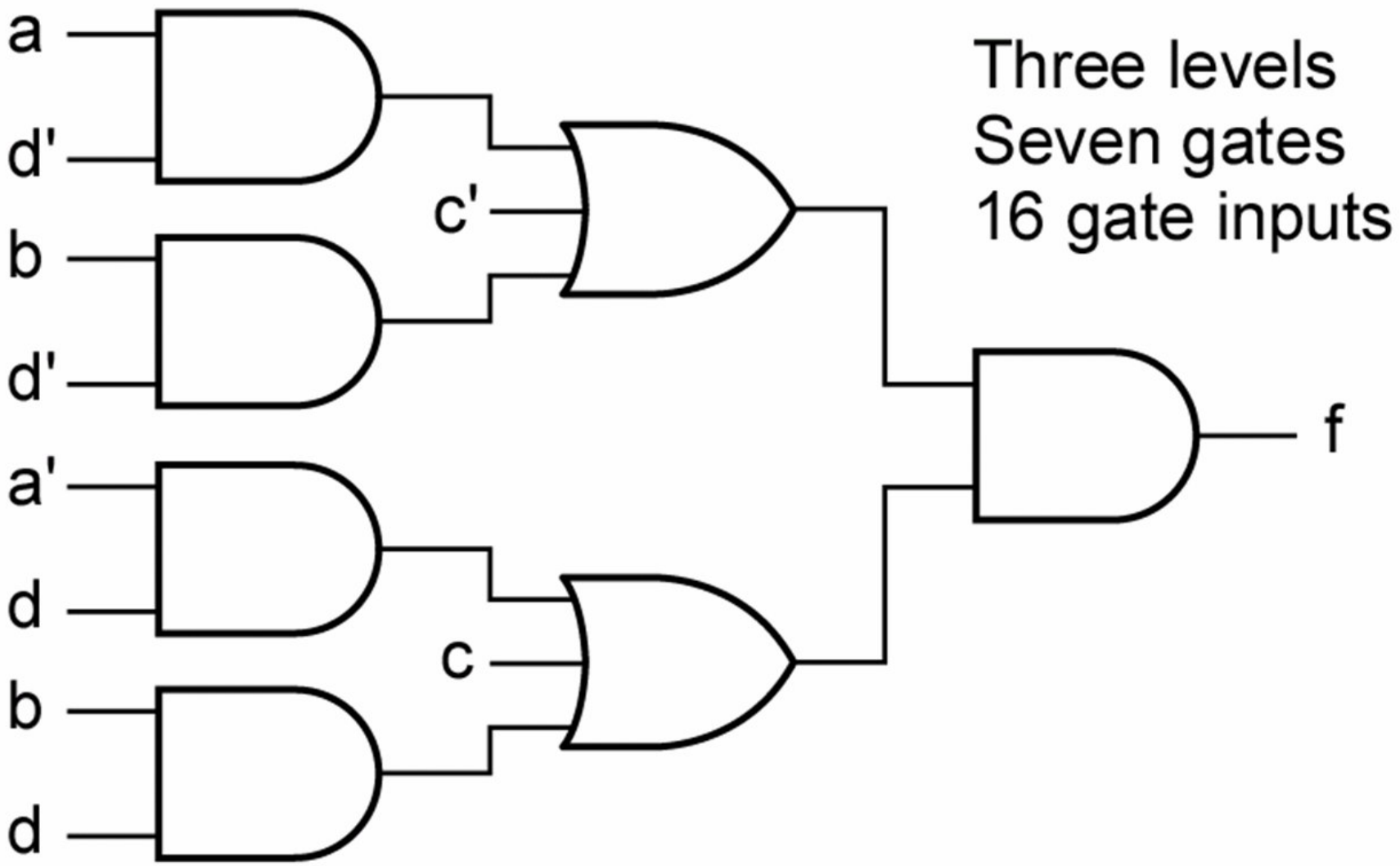
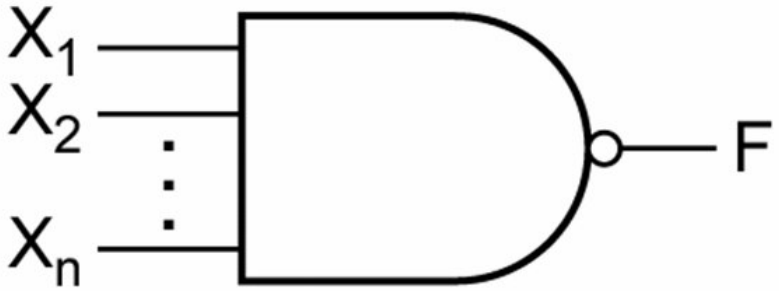


Figure 7-7

(a) 3-input NAND gate

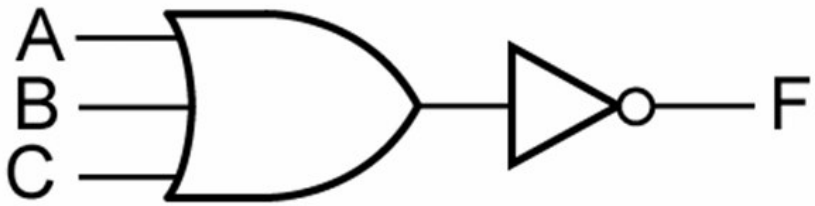
(b) NAND gate equivalent



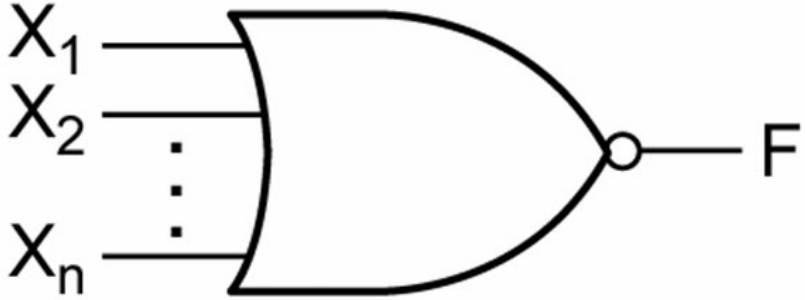
(c) n-input NAND gate

Figure 7-8: **NAND Gates**

(a) 3-input NOR gate

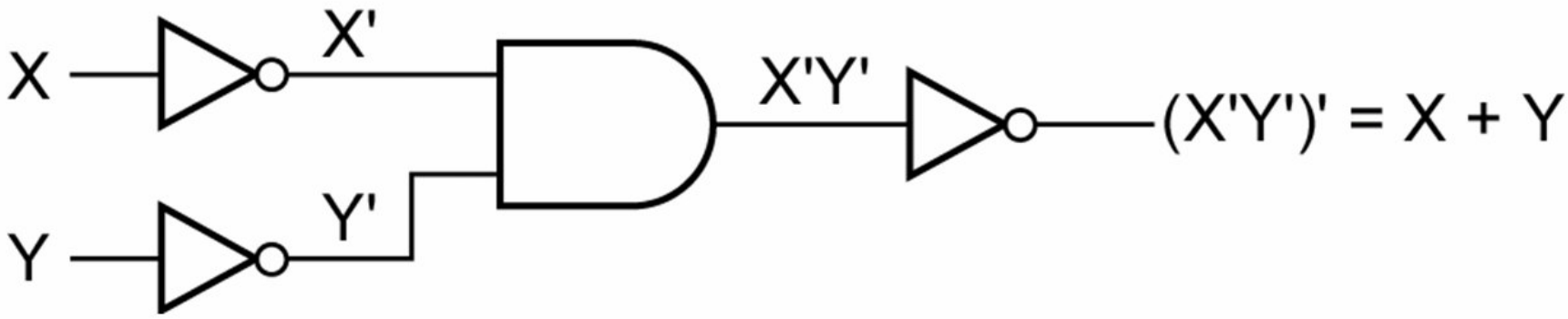


(b) NOR gate equivalent



(c) n-input NOR gate

Figure 7-9: **NOR Gates**



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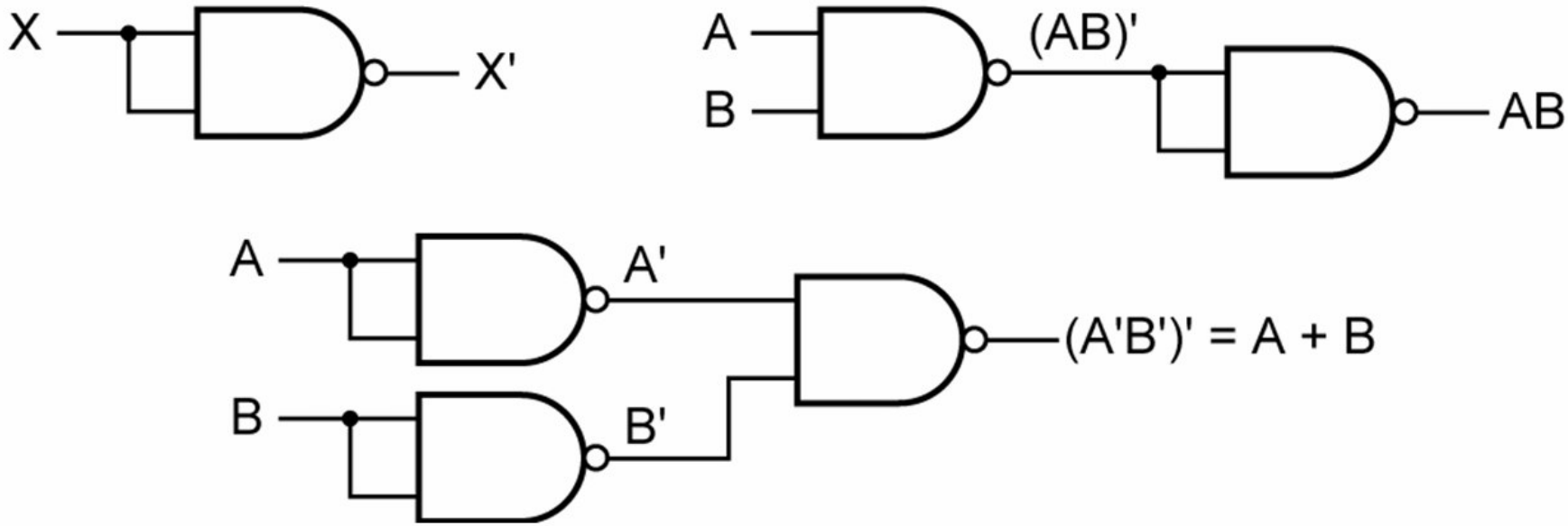


Figure 7-10: **NAND Gate Realization of NOT, AND, and OR**

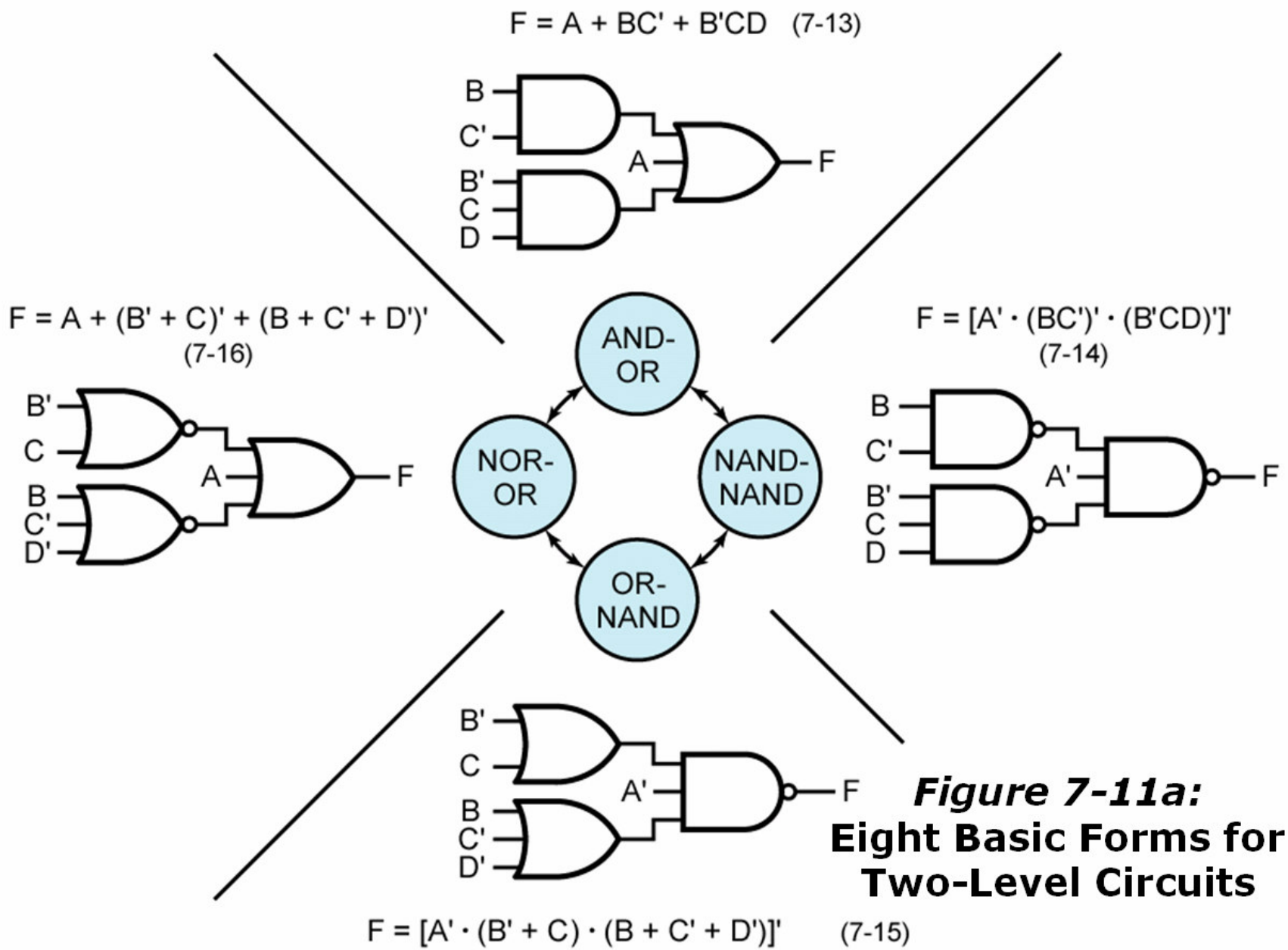


Figure 7-11a:
Eight Basic Forms for Two-Level Circuits

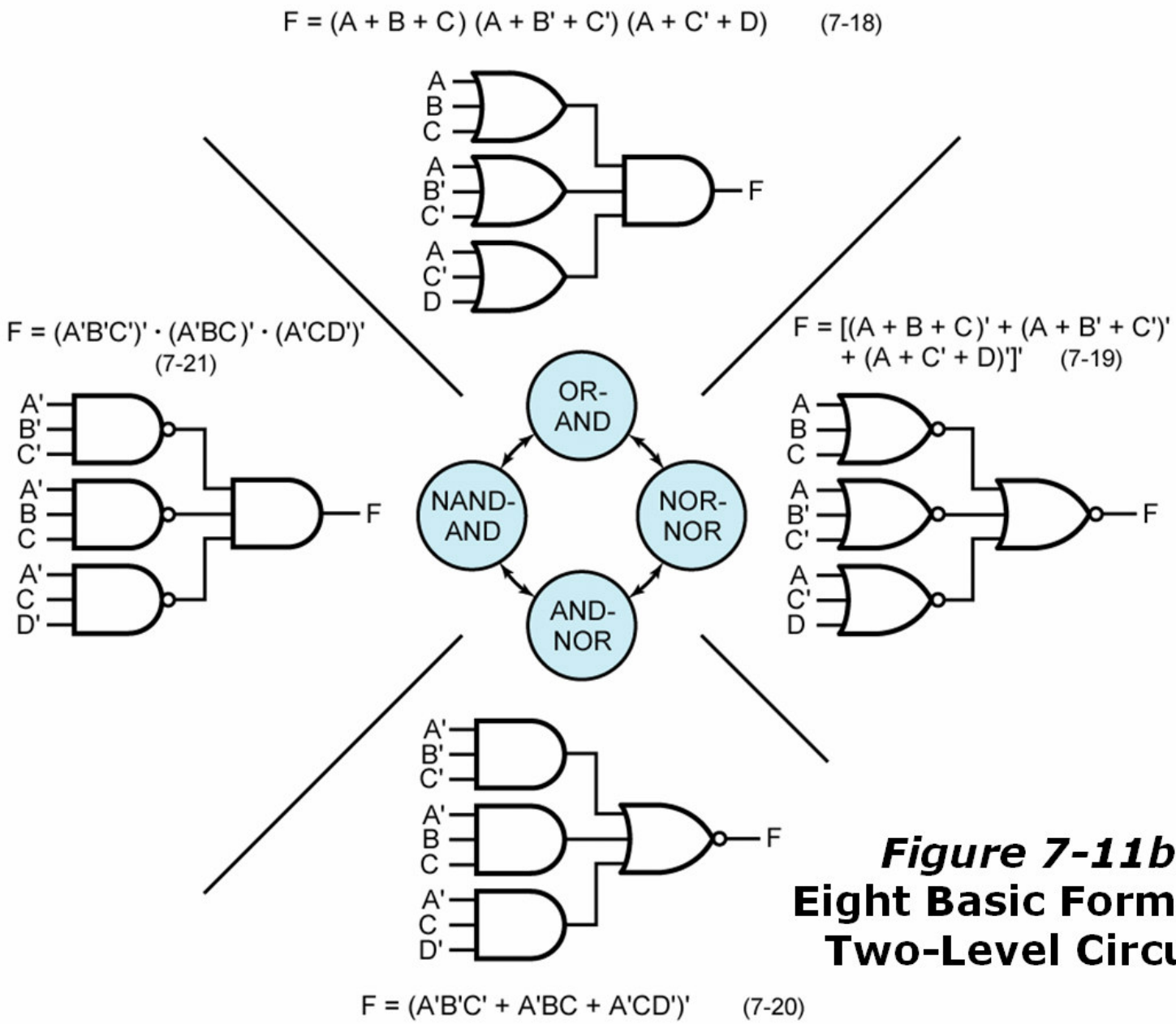
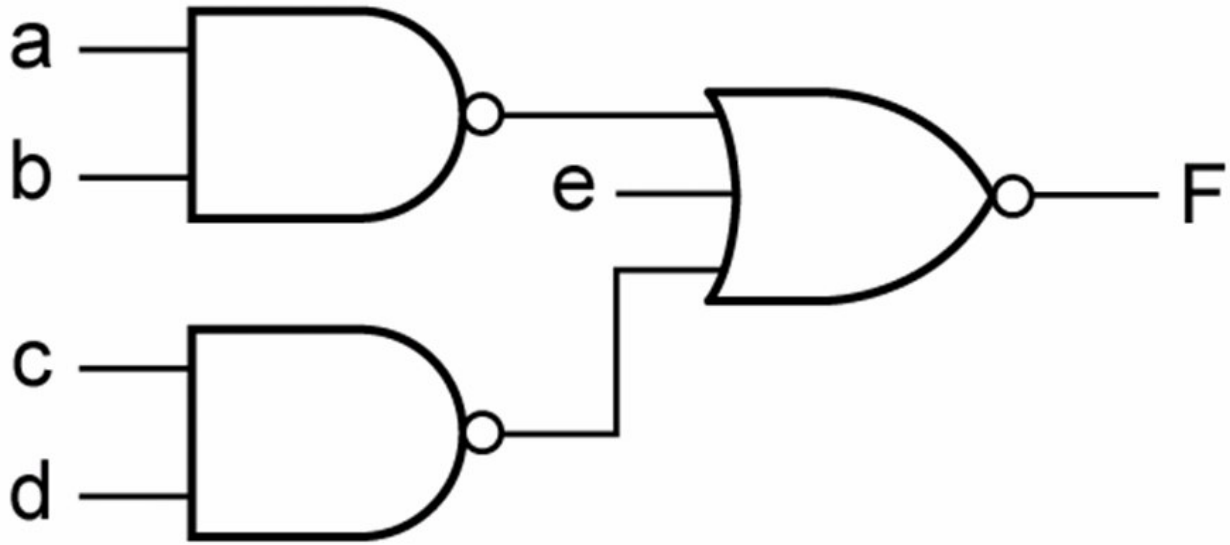


Figure 7-11b:
Eight Basic Forms for Two-Level Circuits



$$F = [(ab)' + (cd)' + e]' = abcde'$$

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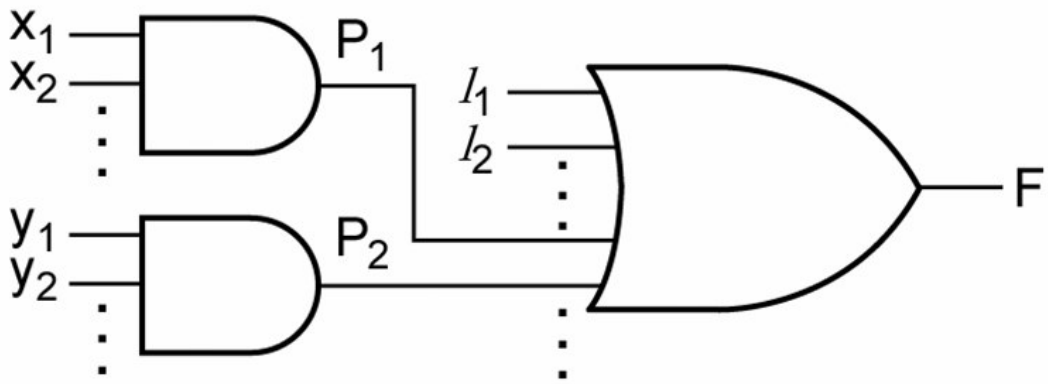
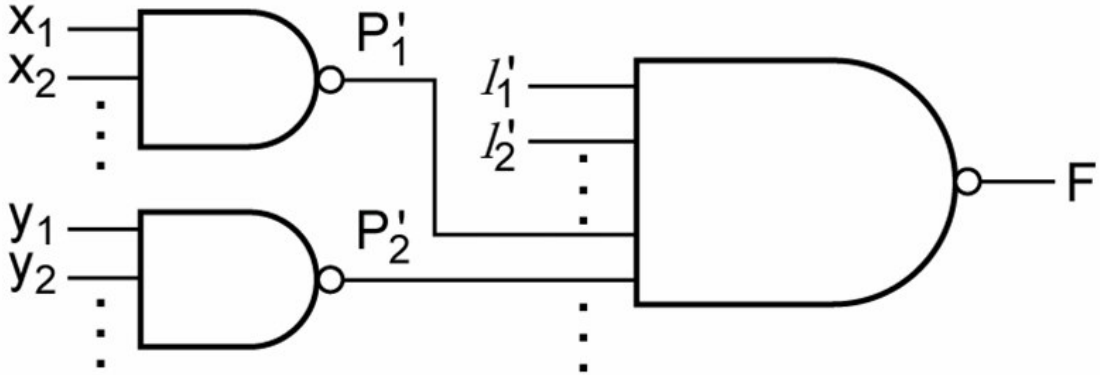
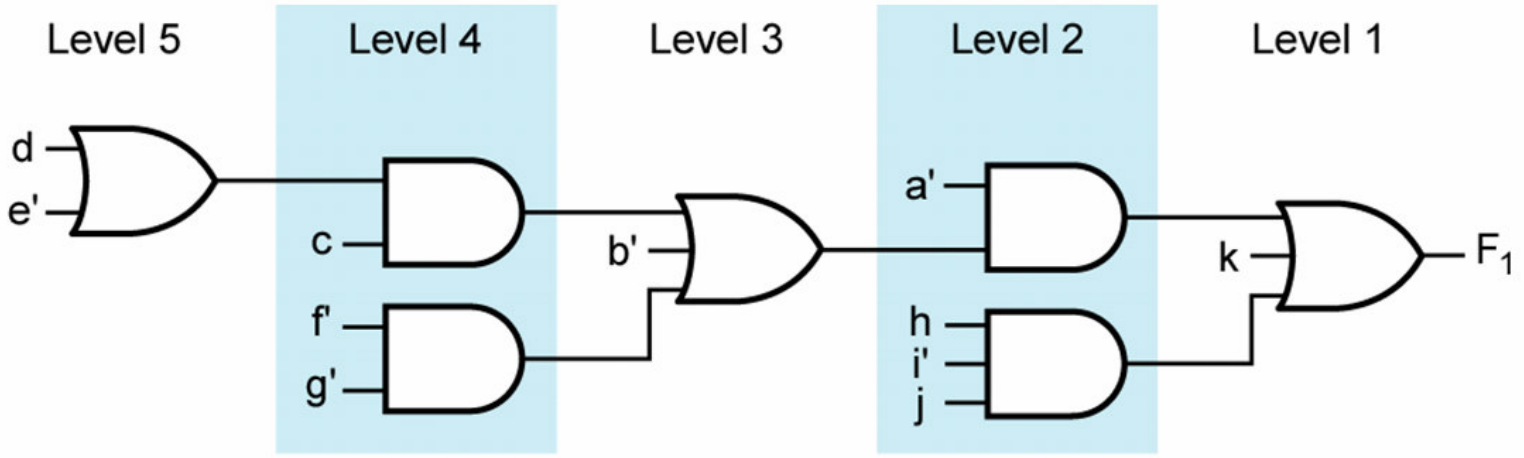


(a) Before transformation

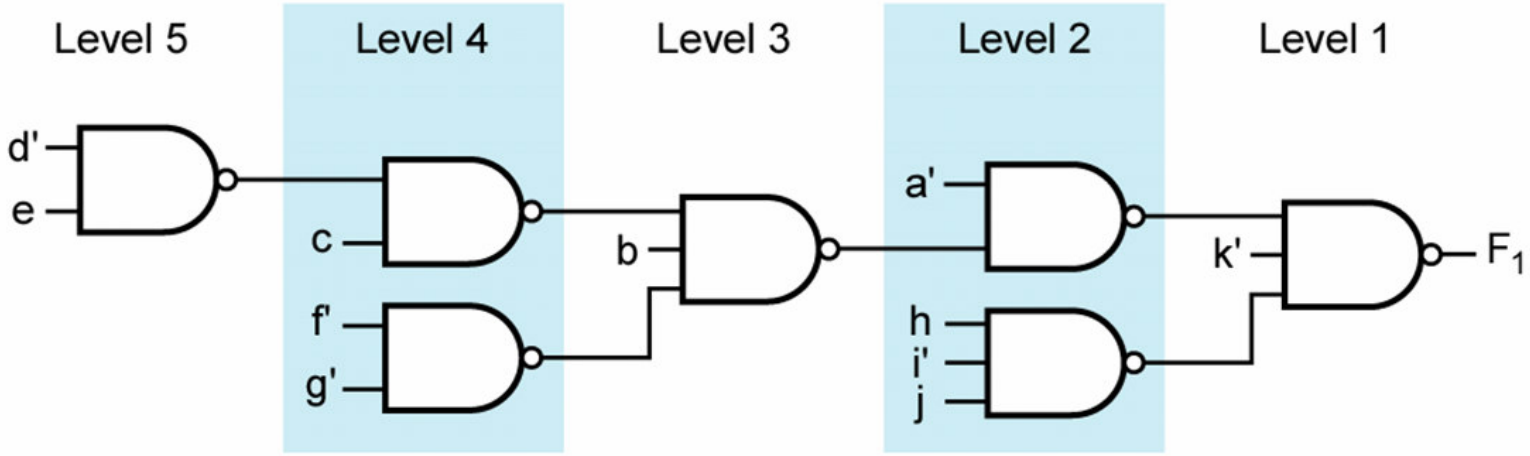


(b) After transformation

Figure 7-12: **AND-OR to NAND-NAND Transformation**

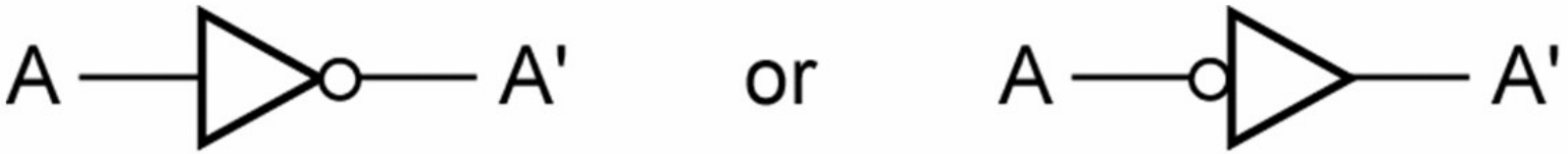


(a) AND-OR network



(b) NAND network

Figure 7-13: **Multi-Level Circuit Conversion to NAND Gates**



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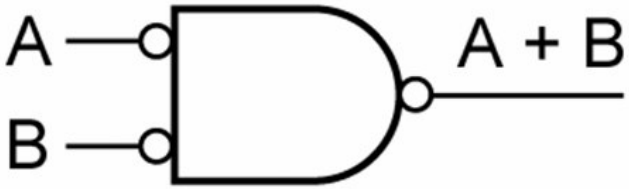
AB = (A' + B')'

(a) AND

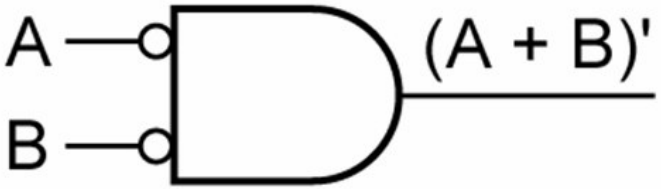


A + B = (A'B')'

(b) OR

(AB)' = A' + B'

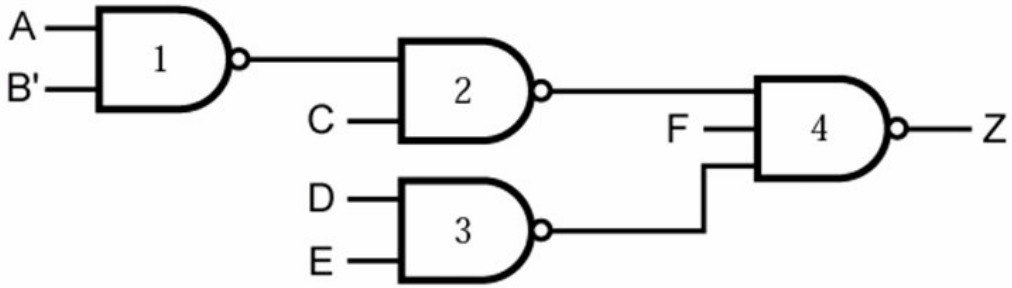
(c) NAND



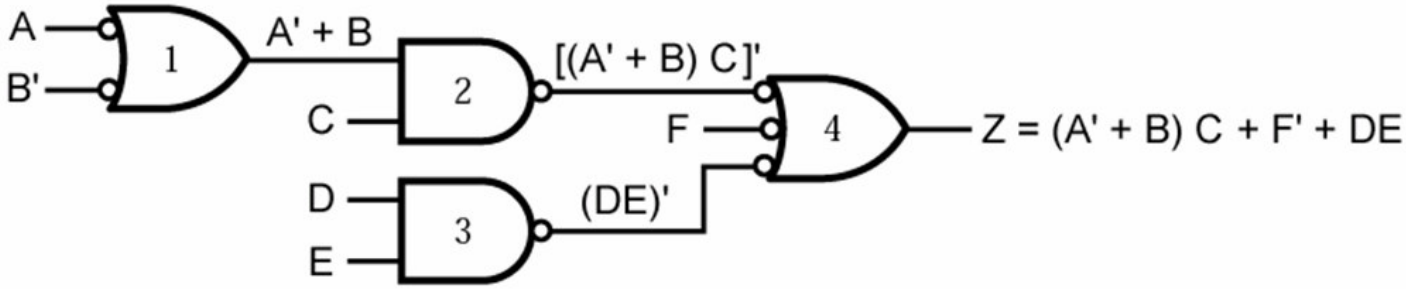
(A + B)' = A'B'

(d) NOR

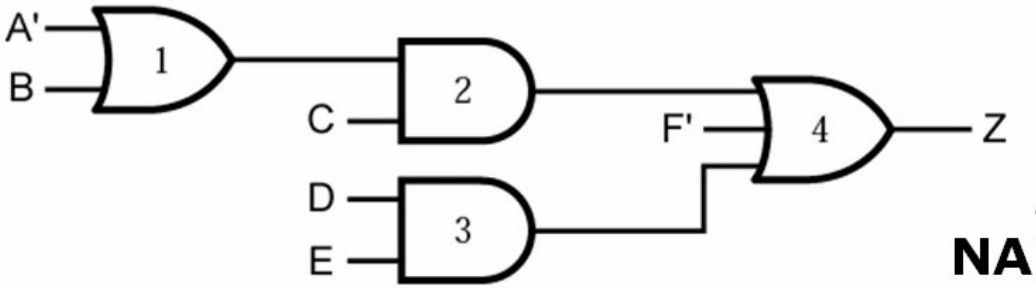
Figure 7-14: **Alternative Gate Symbols**



(a) NAND gate network

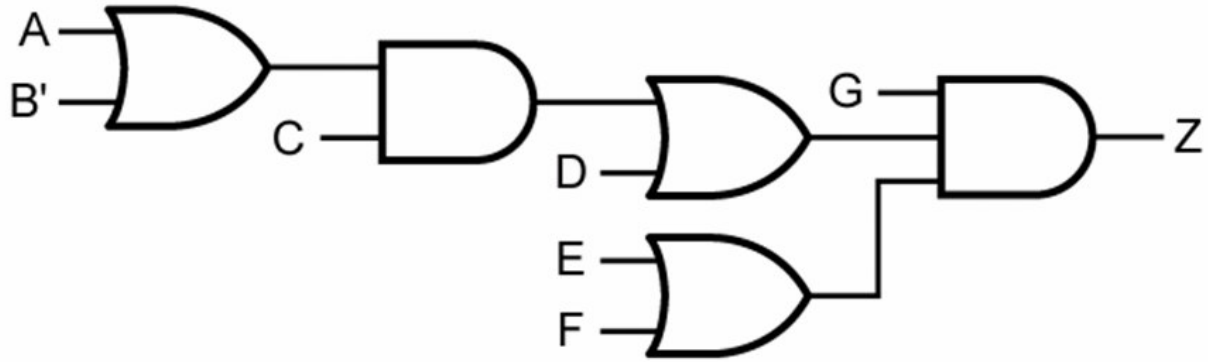


(b) Alternate form for NAND gate network



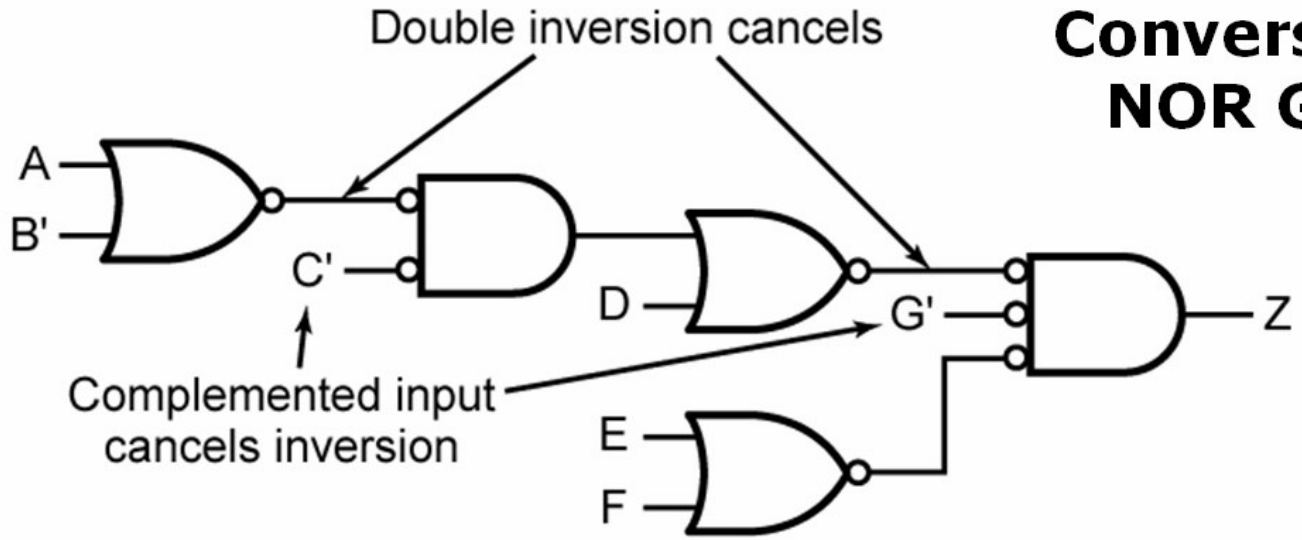
(c) Equivalent AND-OR network

Figure 7-15:
NAND Gate Circuit Conversion

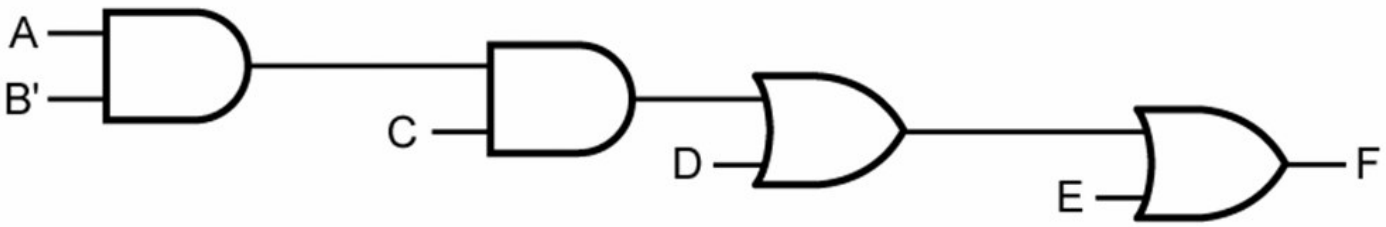


(a) Circuit with OR and AND gates

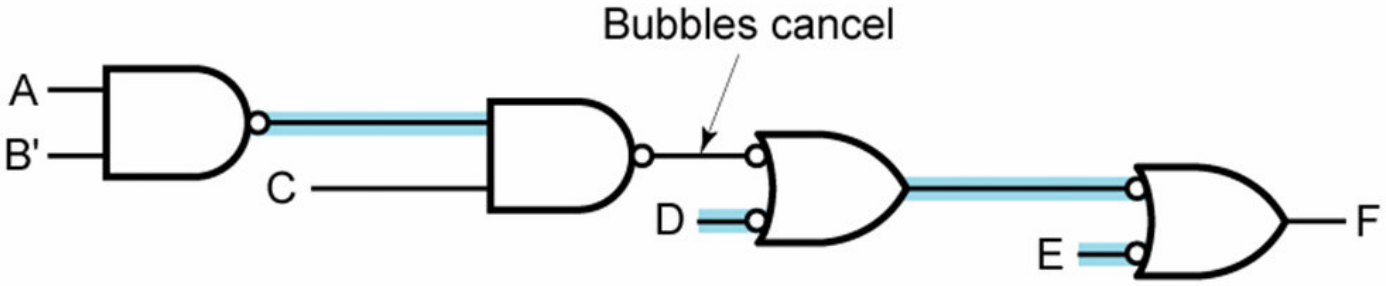
Figure 7-16:
Conversion to NOR Gates



(b) Equivalent circuit with NOR gates

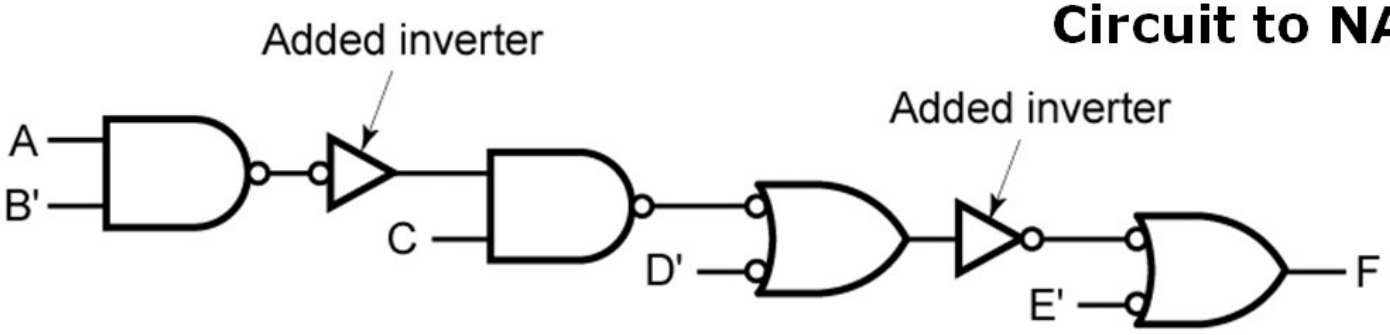


(a) AND-OR network

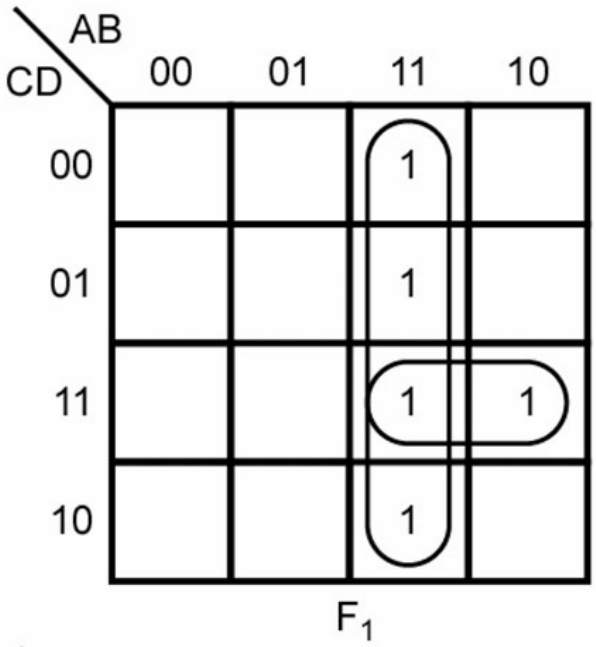


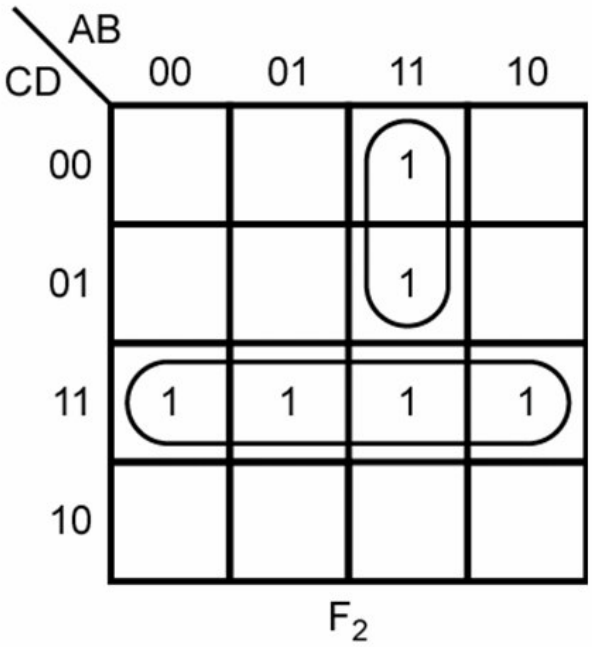
(b) First step in NAND conversion

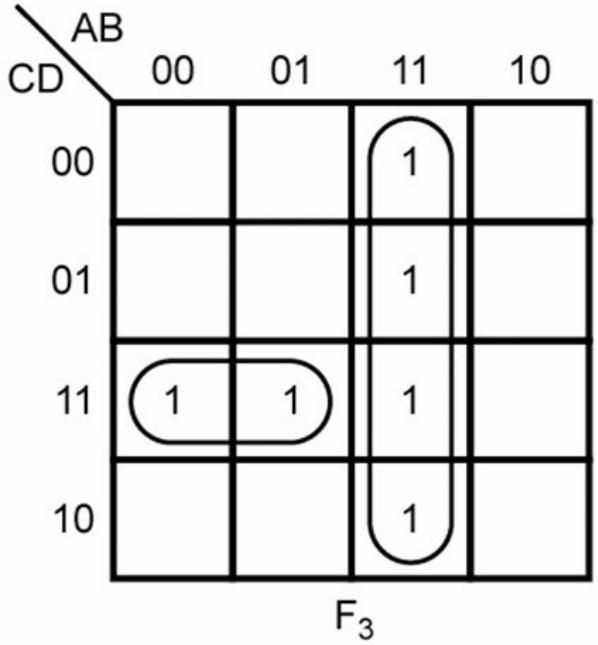
Figure 7-17:
Conversion of AND-OR Circuit to NAND Gates



(c) Completed conversion







$$F_1(A, B, C, D) = \sum m(11, 12, 13, 14, 15)$$
$$F_2(A, B, C, D) = \sum m(3, 7, 11, 12, 13, 15)$$
$$F_3(A, B, C, D) = \sum m(3, 7, 12, 13, 14, 15)$$

Figure 7-18: **Karnaugh Maps for Equations (7-22)**

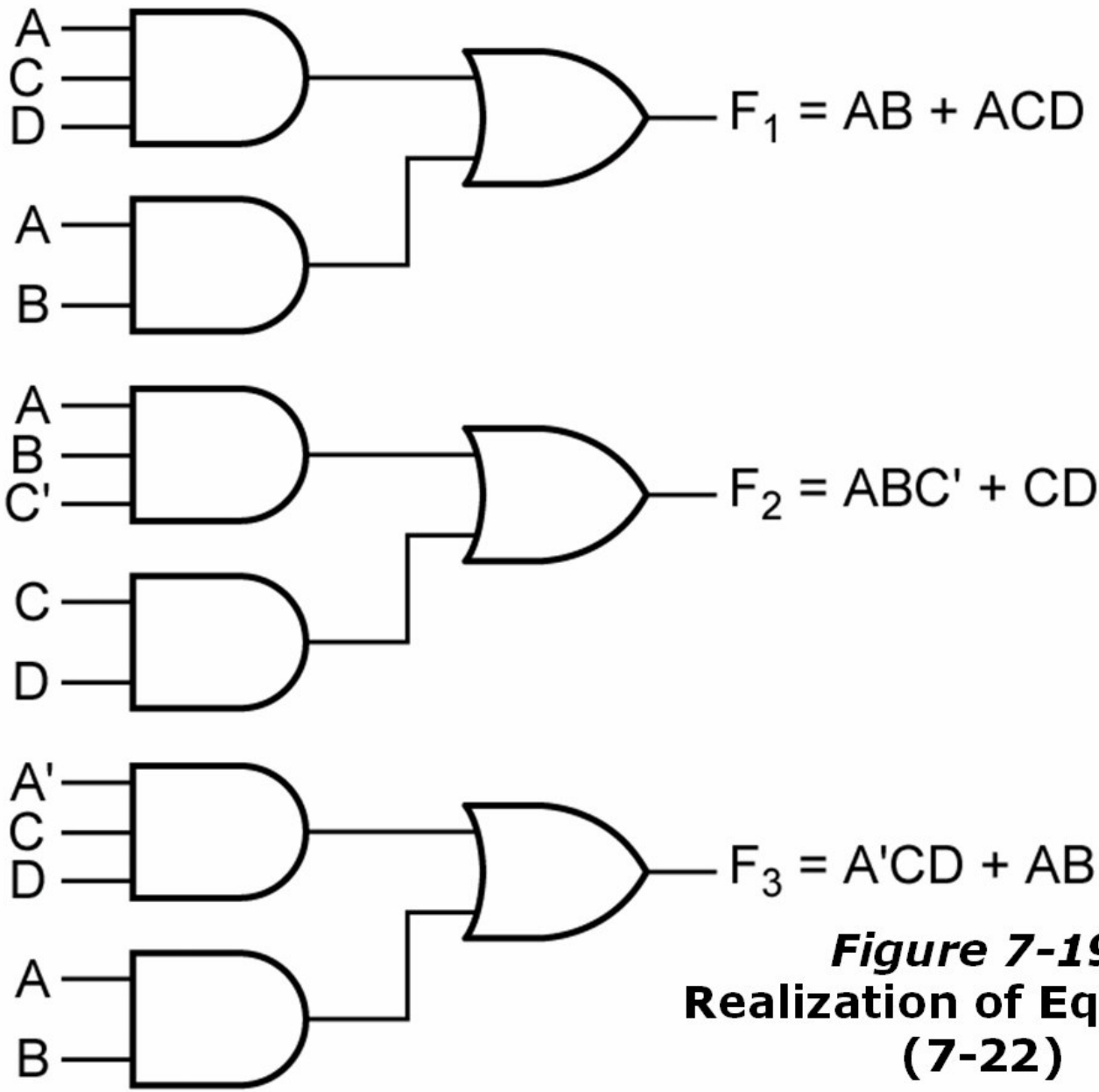


Figure 7-19:
Realization of Equations (7-22)

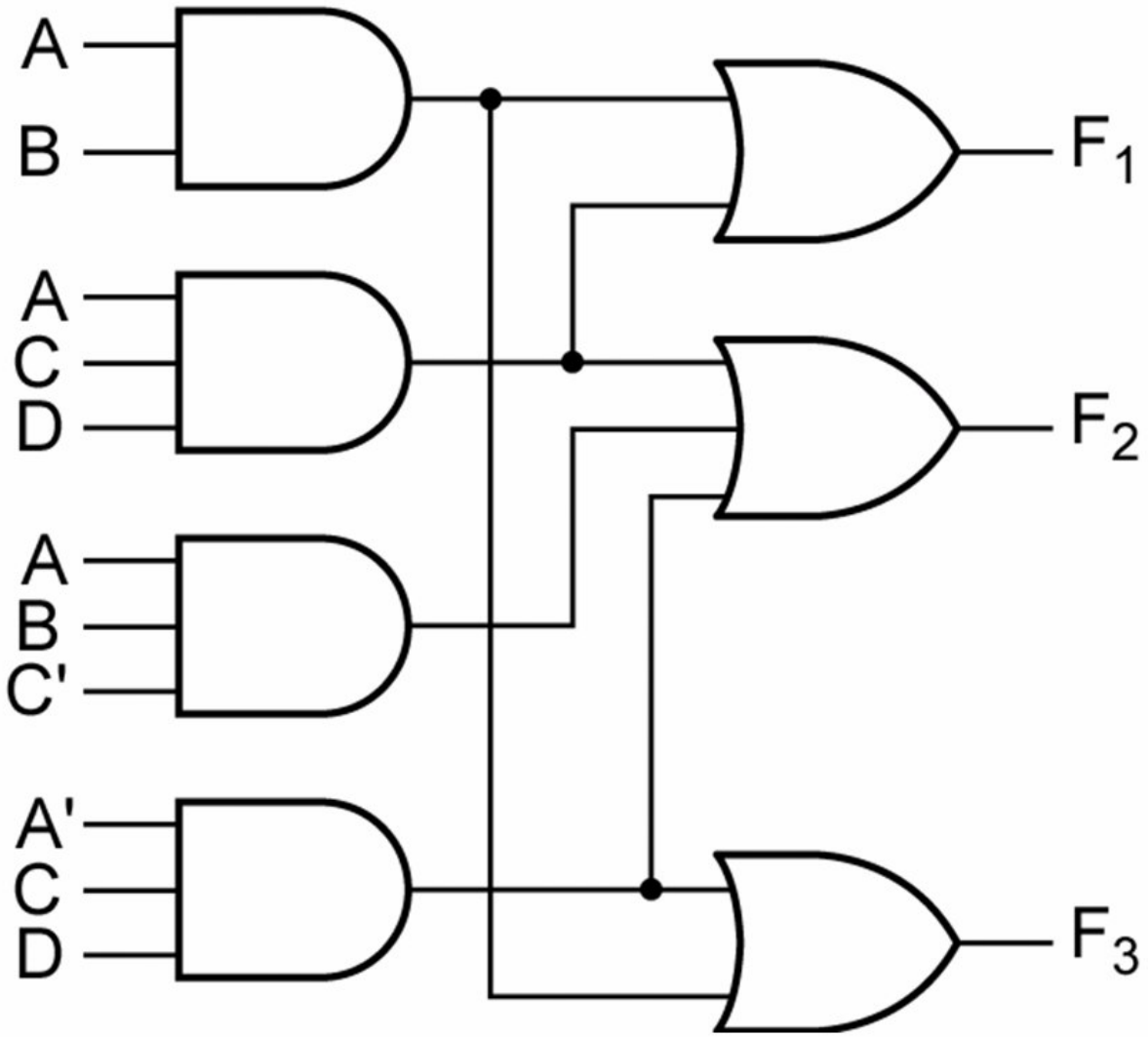


Figure 7-20: **Multiple-Output Realization of Equations (7-22)**

$$f_1 = \sum m(2, 3, 5, 7, 8, 9, 10, 11, 13, 15)$$
$$f_2 = \sum m(2, 3, 5, 6, 7, 10, 11, 14, 15)$$
$$f_3 = \sum m(6, 7, 8, 9, 13, 14, 15)$$

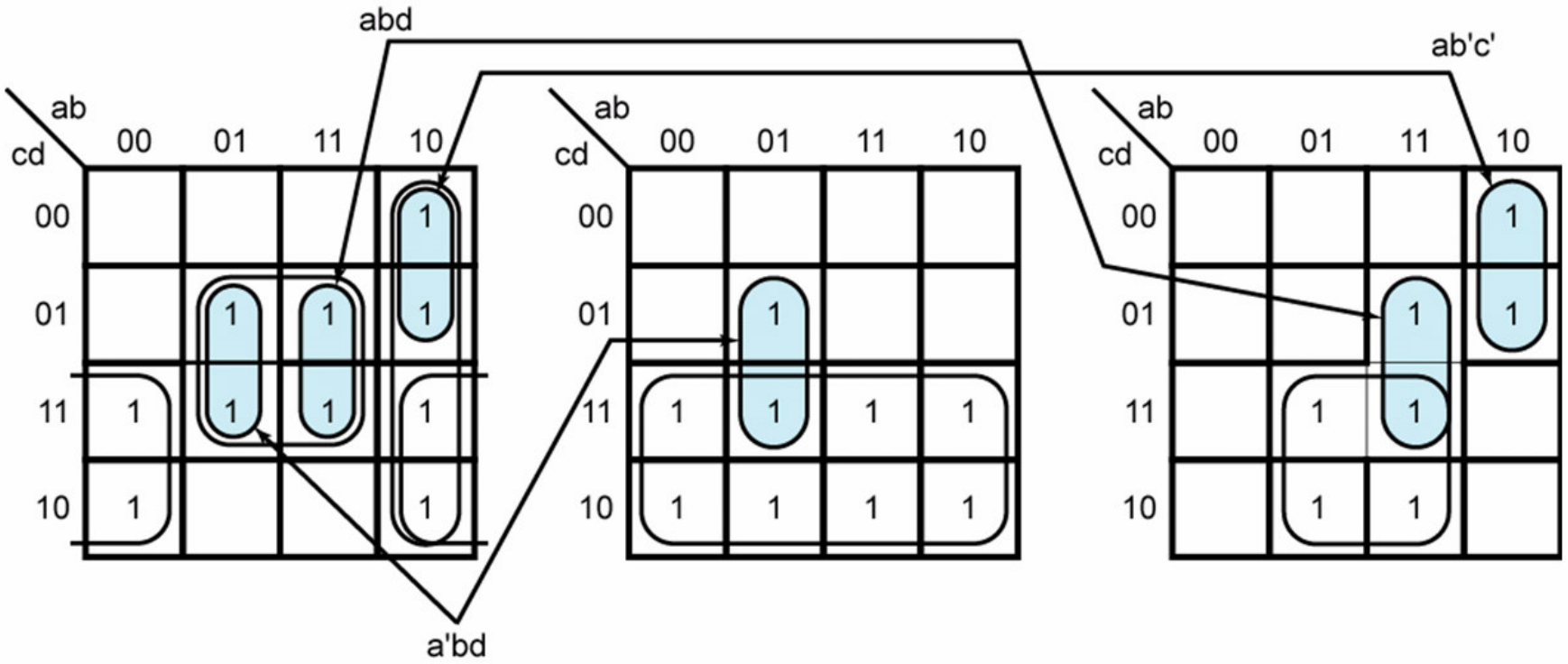
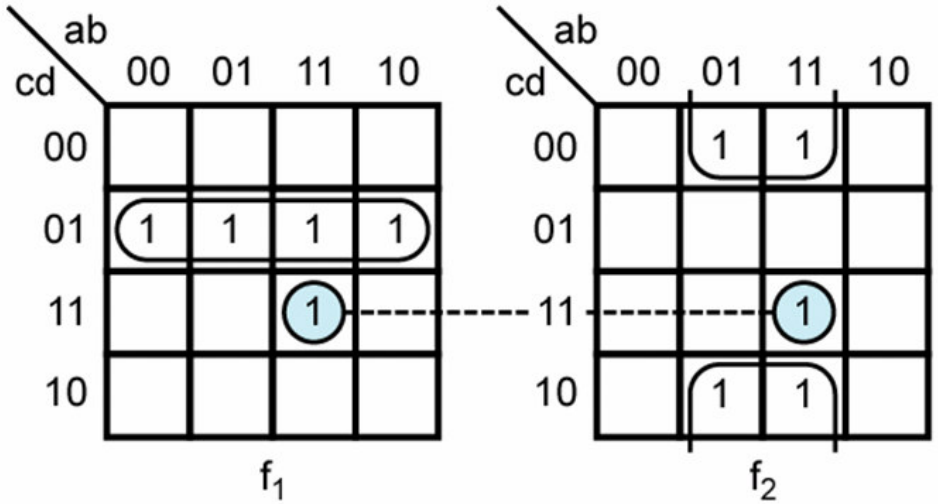
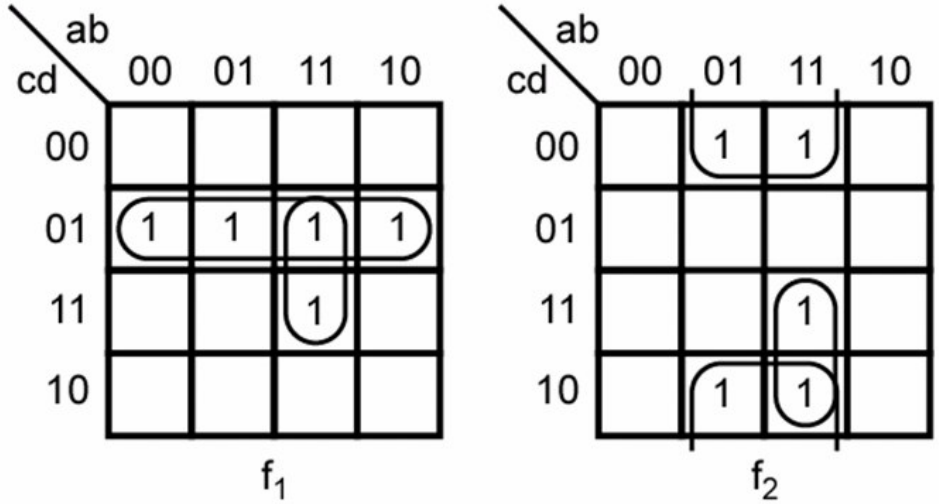


Figure 7-21

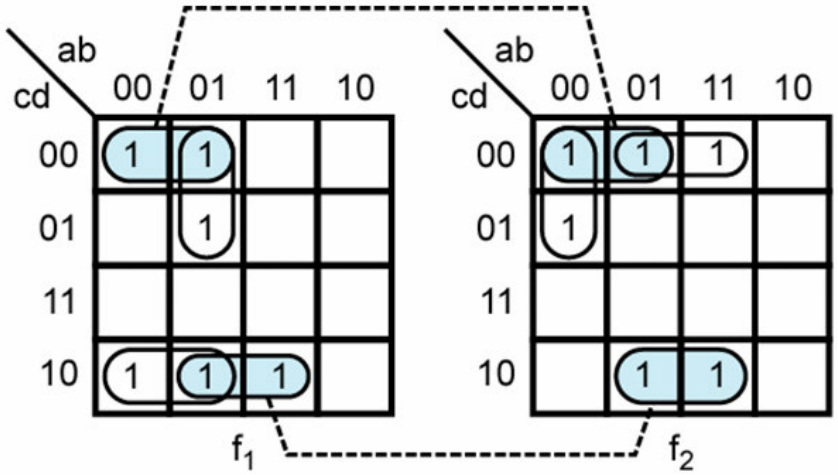


(a) Best solution

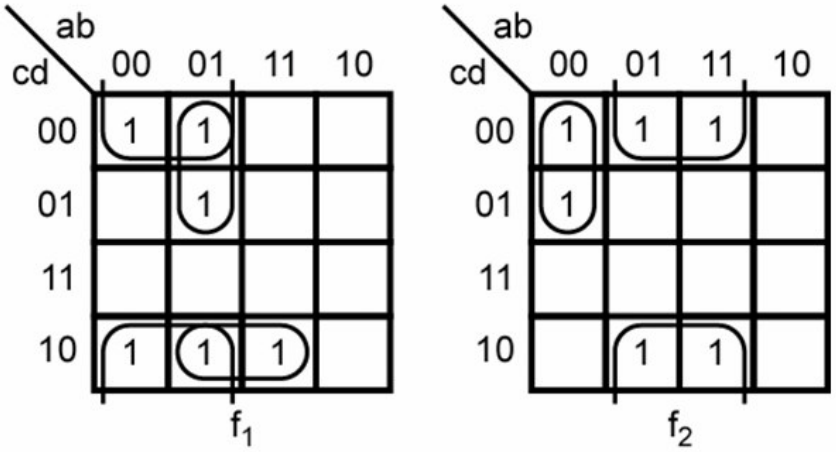


(b) Solution requires an extra gate

Figure 7-22

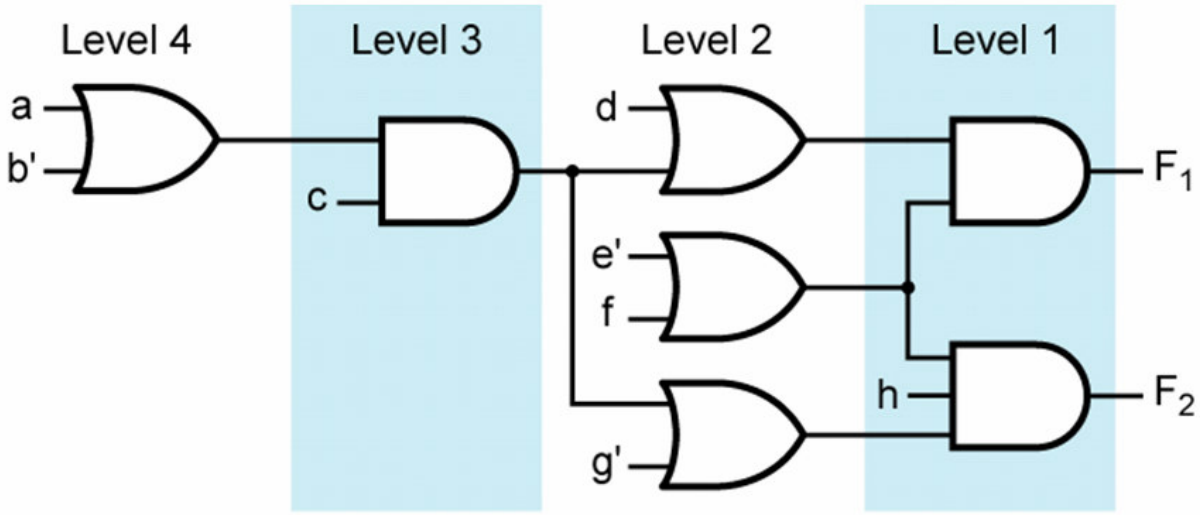


(a) Solution with maximum number of common terms requires 8 gates, 26 inputs

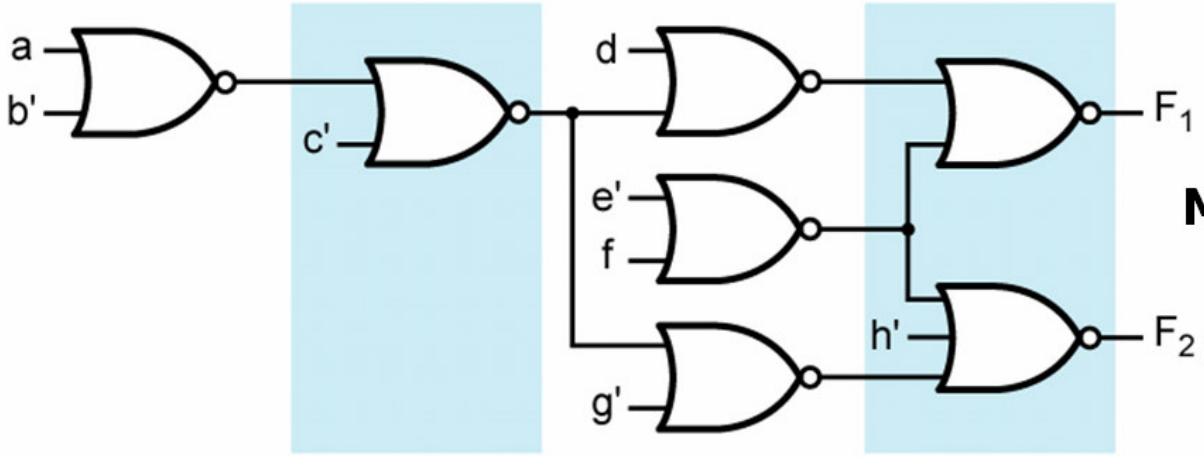


(b) Best solution requires 7 gates, 18 inputs and has no common terms

Figure 7-23



(a) Network of AND and OR gates



(b) NOR network

Figure 7-24:
Multi-Level Circuit Conversion to NOR Gates