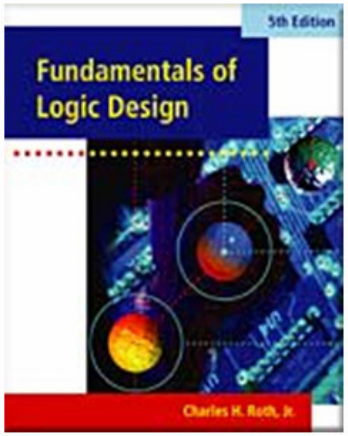
FIGURES FOR

CHAPTER 18

CIRCUITS FOR ARITHMETIC OPERATIONS



This chapter in the book includes:

Objectives
Study Guide
18.1 Serial Adder with Accumulator
18.2 Design of a Parallel Multiplier
18.3 Design of a Binary Divider
Programmed Exercises
Problems

Click the mouse to move to the next page.
Use the ESC key to exit this chapter.

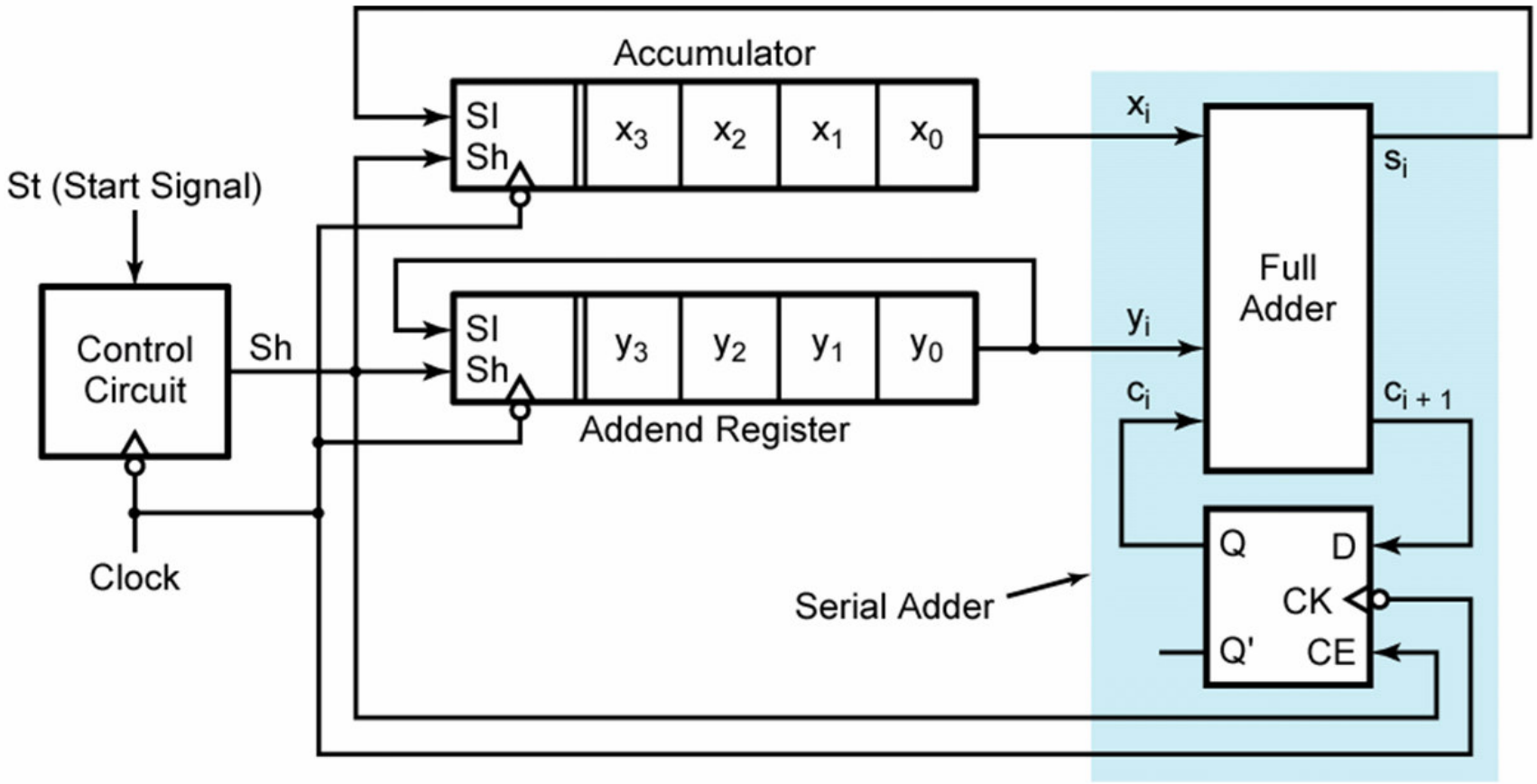


Figure 18-1: **Block Diagram for Serial Adder with Accumulator**

Figure 18-2ab:
Operation of Serial Adder

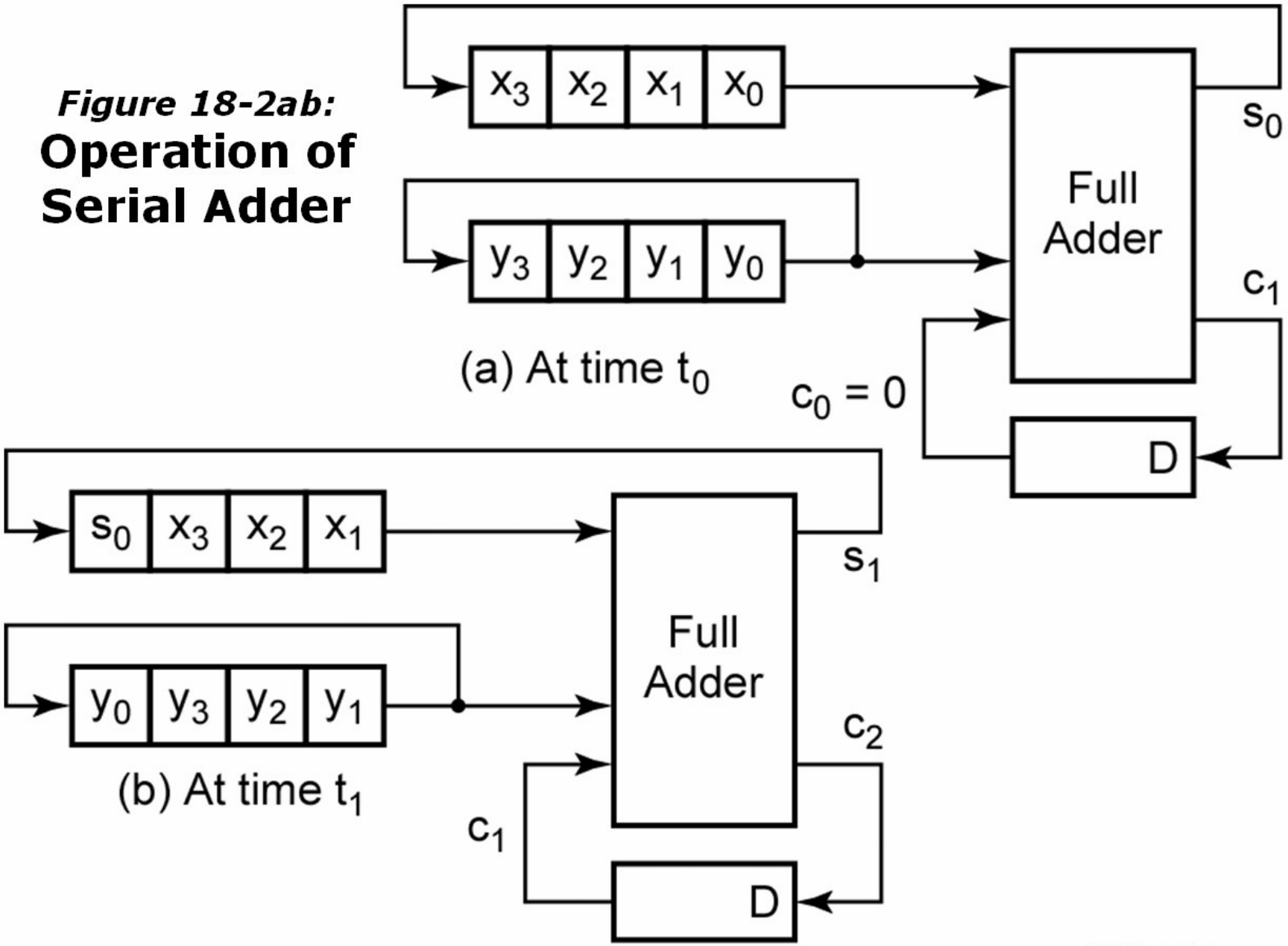
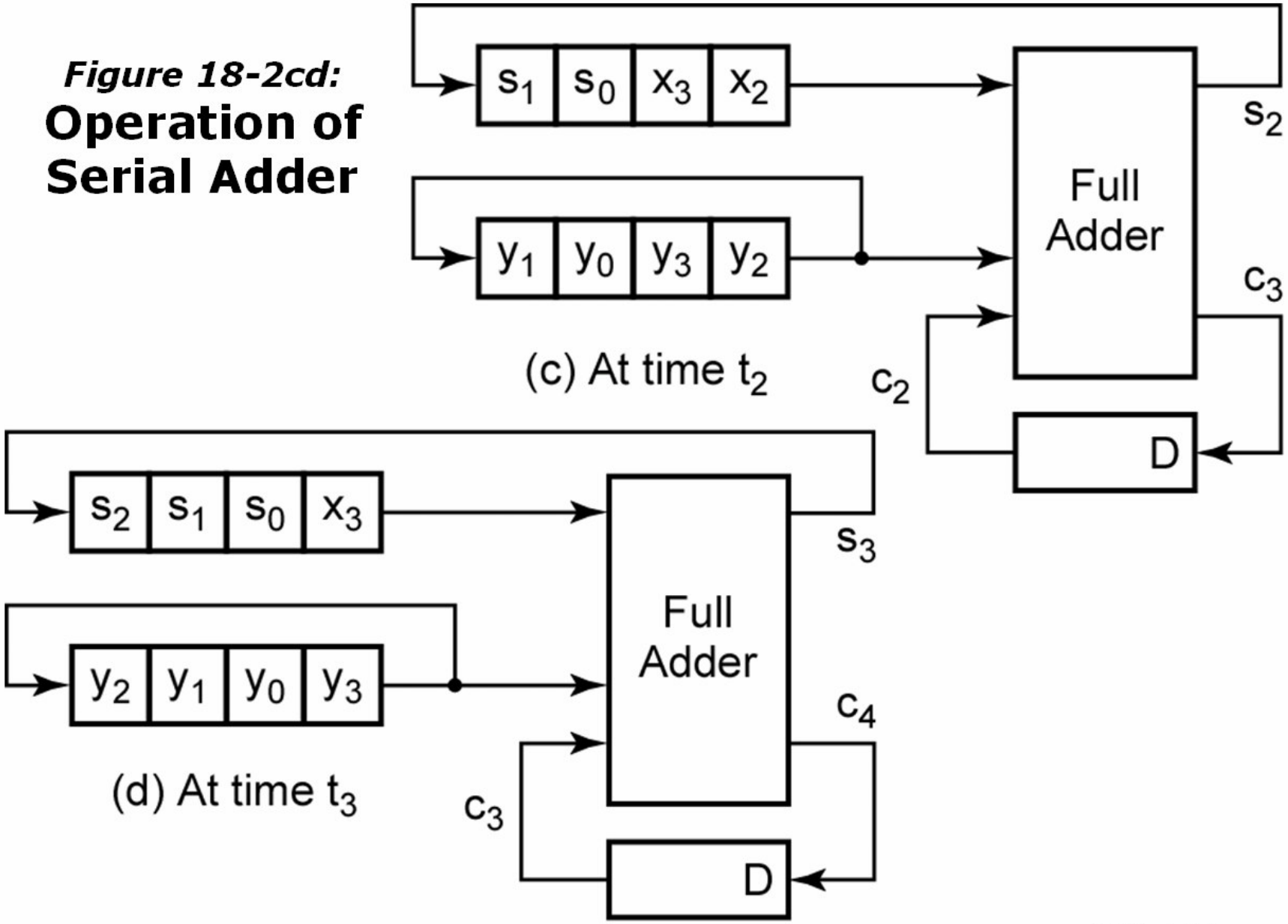
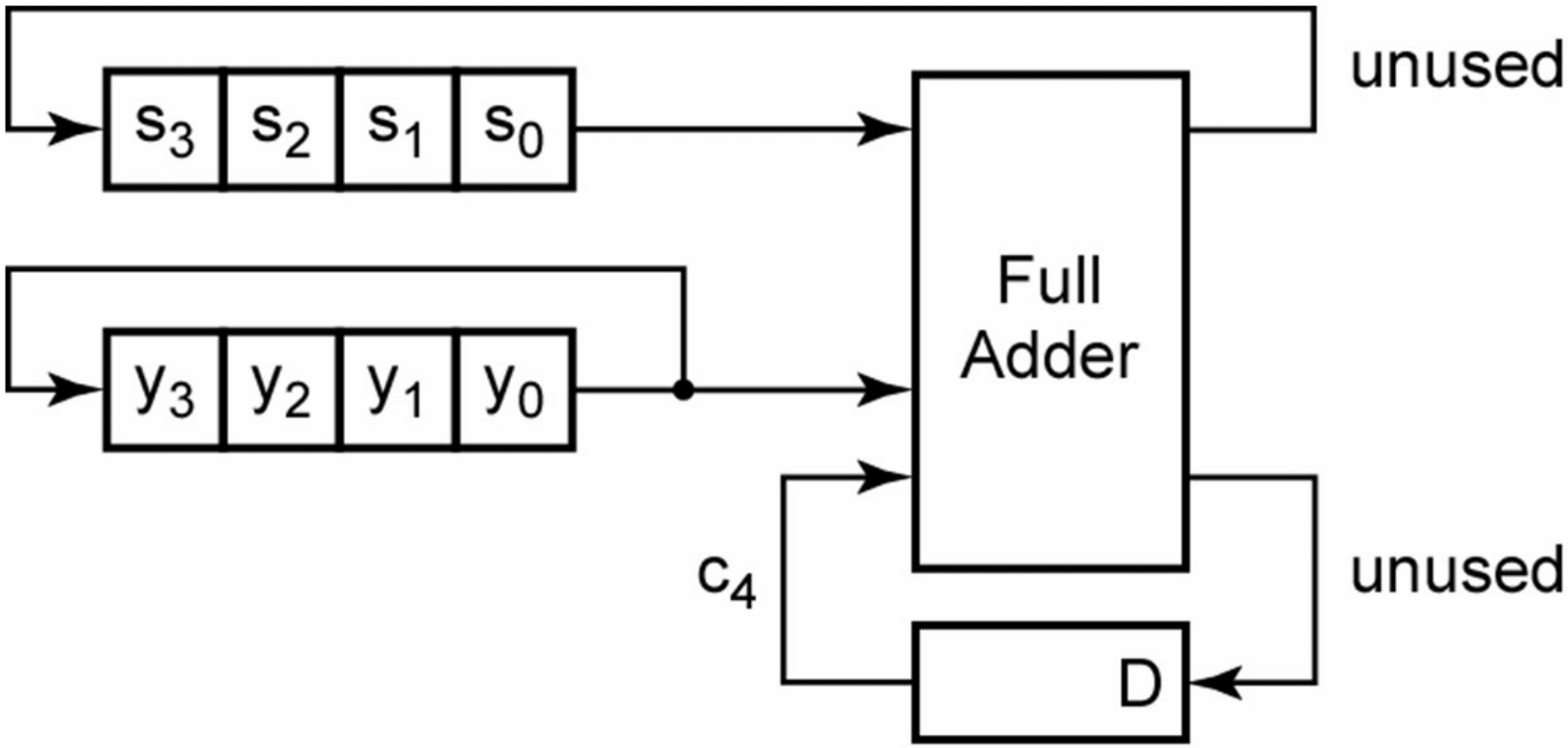


Figure 18-2cd:
Operation of Serial Adder



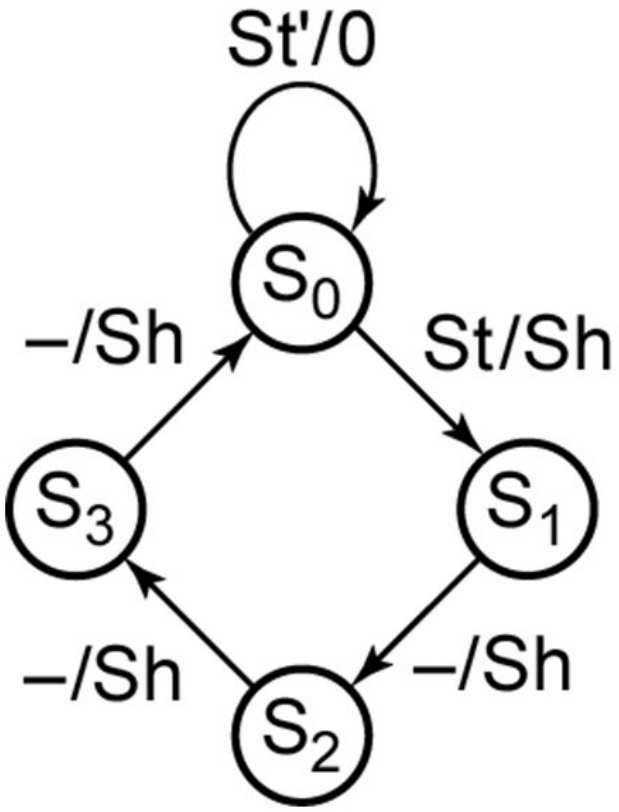


(e) At time t_4

Figure 18-2c:
Operation of Serial Adder

Table 18-1 Operation of Serial Adder

	X	Y	c_i	s_i	c_i^+
t_0	0101	0111	0	0	1
t_1	0010	1011	1	0	1
t_2	0001	1101	1	1	1
t_3	1000	1110	1	1	0
t_4	1100	0111	0	(1)	(0)



	Next State		Sh	
	St = 0	1	0	1
S_0	S_0	S_1	0	1
S_1	S_2	S_2	1	1
S_2	S_3	S_3	1	1
S_3	S_0	S_0	1	1

Figure 18-3: **State Graph for Serial Adder Control**

	AB	A^+B^+	
		0	1
S_0	00	00	01
S_1	01	10	10
S_2	10	11	11
S_3	11	00	00

Figure 18-4a: **Derivation of Control Circuit Equations**

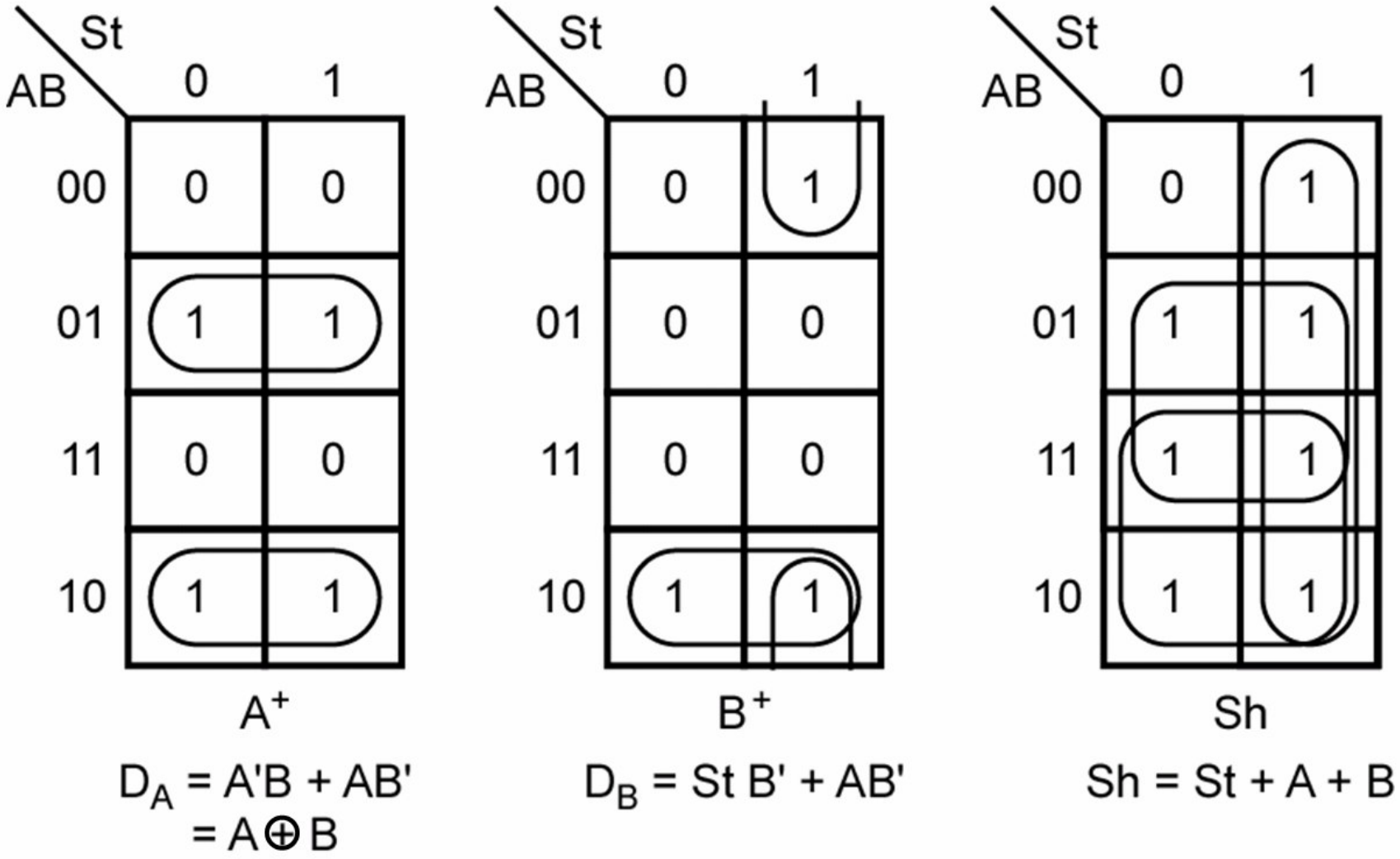


Figure 18-4b: **Derivation of Control Circuit Equations**

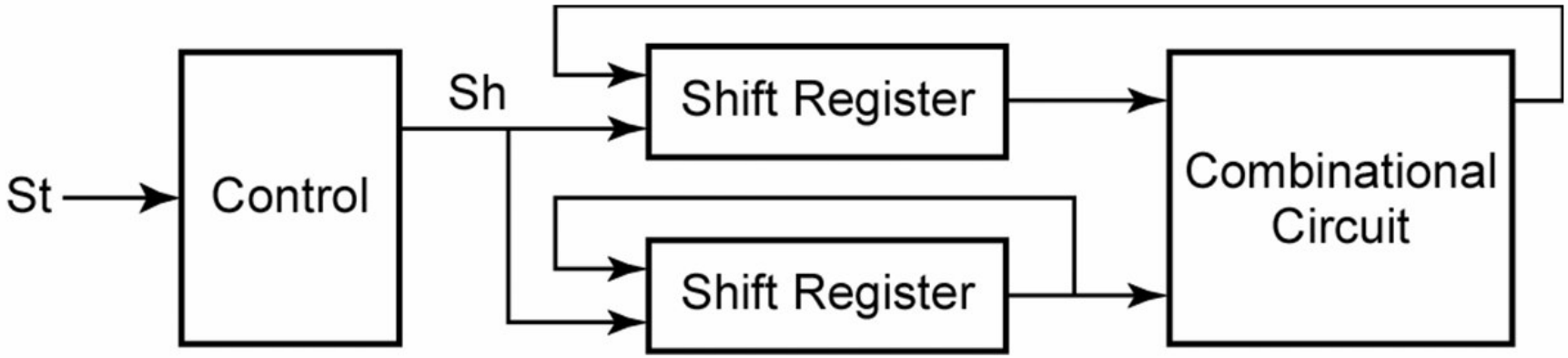


Figure 18-5: **Typical Serial Processing Unit**

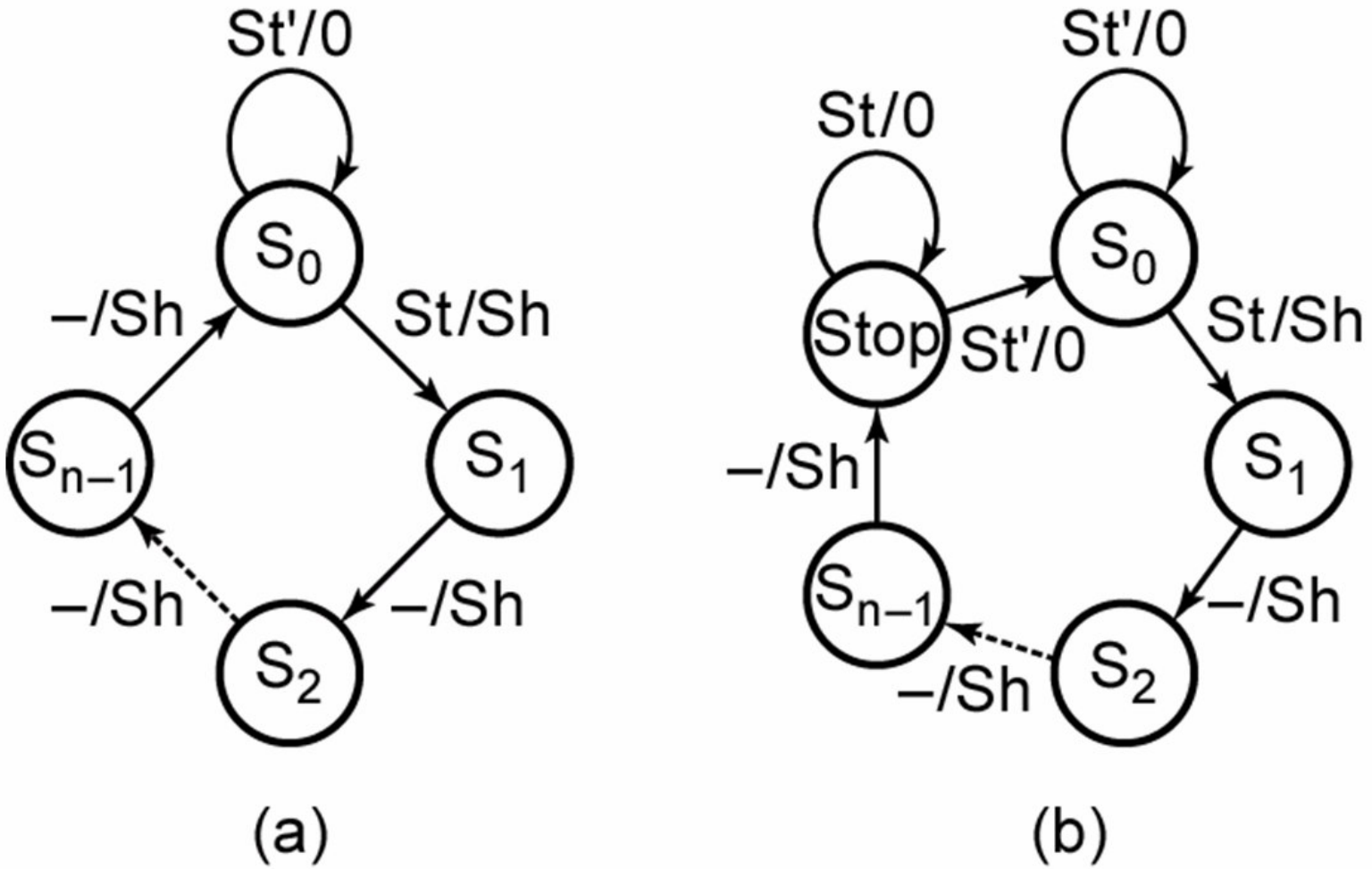


Figure 18-6: **State Graphs for Serial Processing Unit**

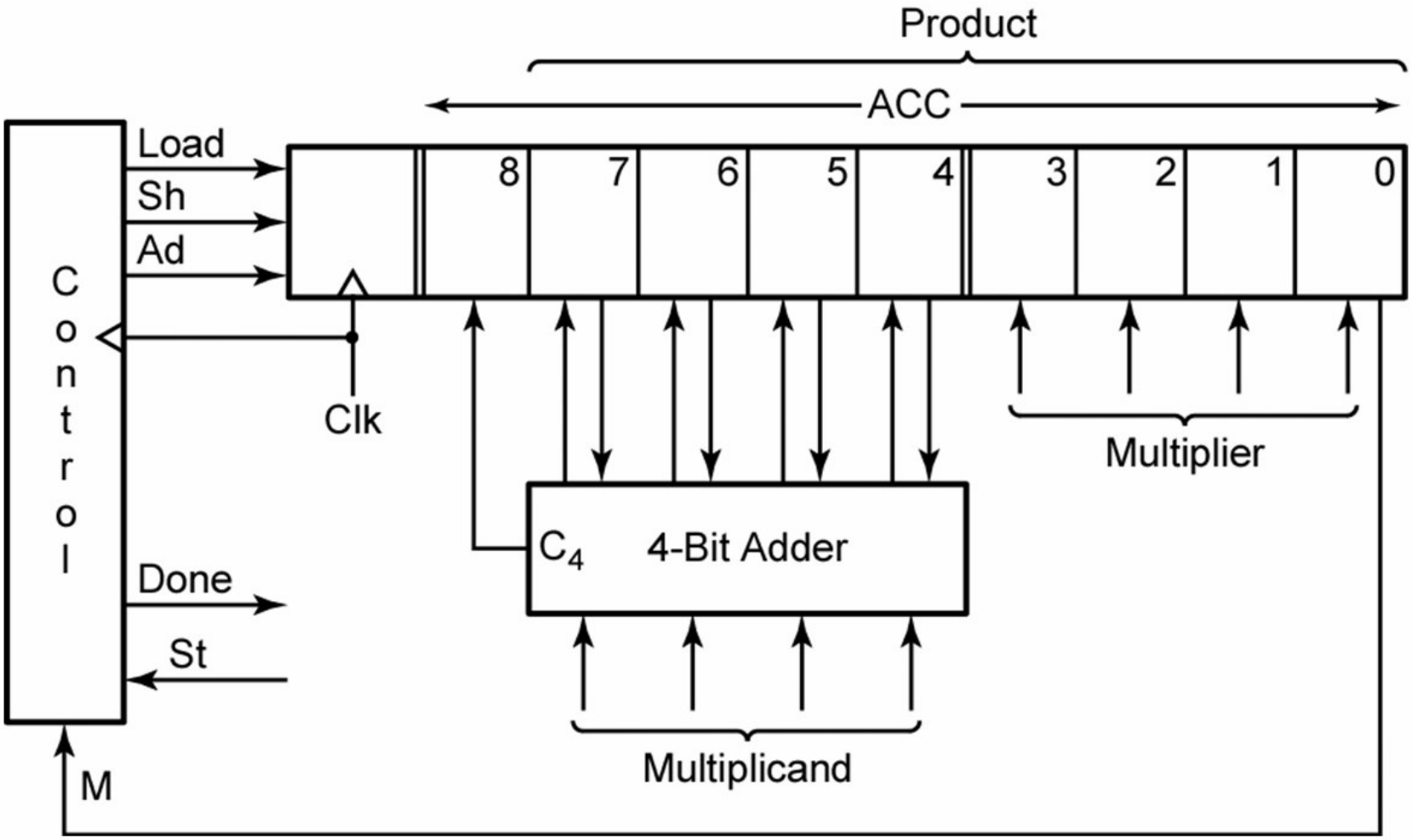


Figure 18-7: **Block Diagram for Parallel Binary Multiplier**

Parallel Binary Multiplication

initial contents of product register	0 0 0 0 0 | 1 0 1 1 $\leftarrow M$	(11)
(add multiplicand since $M = 1$)	1 1 0 1 |	(13)
after addition	0 1 1 0 1 | 1 0 1 1	
after shift	0 0 1 1 0 1 | 1 0 1 $\leftarrow M$	
(add multiplicand since $M = 1$)	1 1 0 1 |	
after addition	1 0 0 1 1 1 | 1 0 1	
after shift	0 1 0 0 1 1 1 | 1 0 $\leftarrow M$	
(skip addition since $M = 0$)	|	
after shift	0 0 1 0 0 1 1 1 | 1 $\leftarrow M$	
(add multiplicand since $M = 1$)	1 1 0 1 |	
after addition	1 0 0 0 1 1 1 1 | 1	
after shift (final answer)	0 1 0 0 0 1 1 1 | 1	(143)

dividing line between product and multiplier

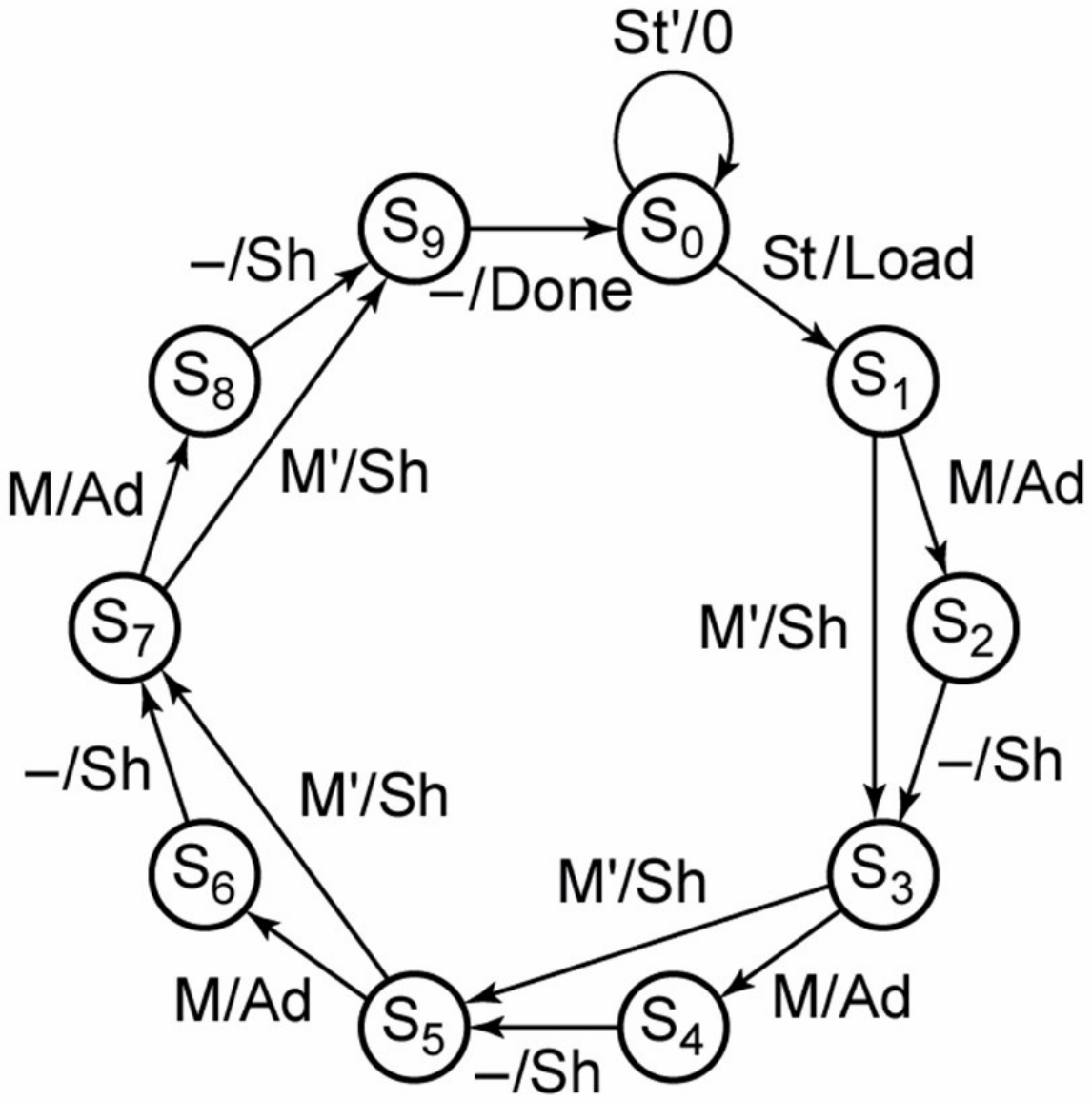
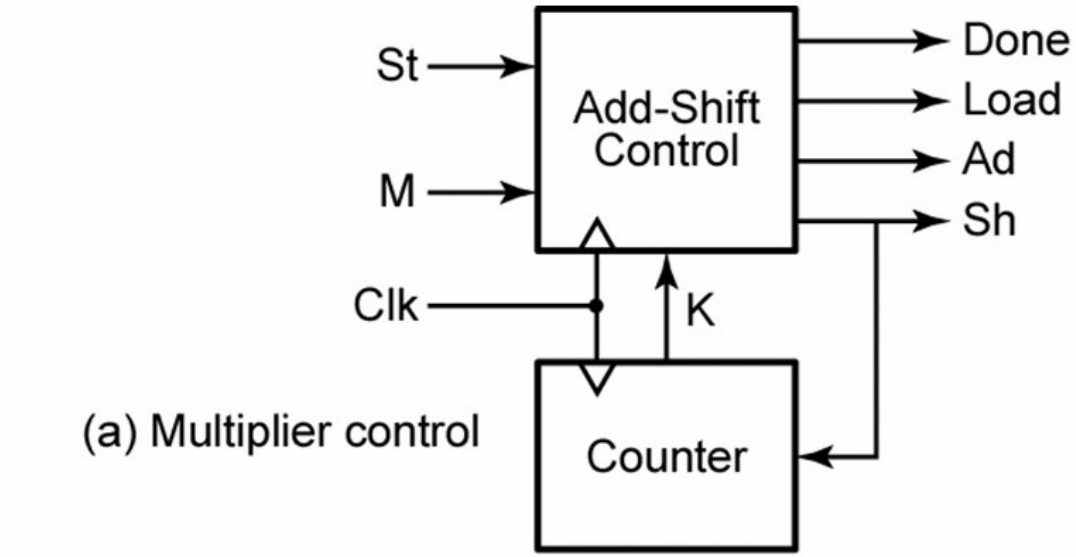
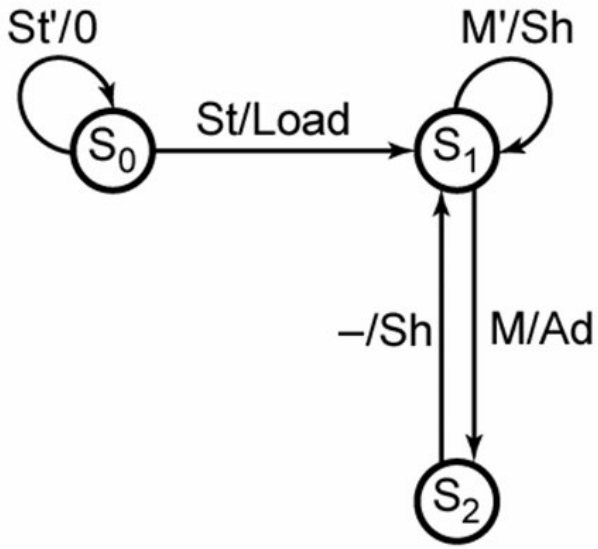


Figure 18-8: **State Graph for Multiplier Control**

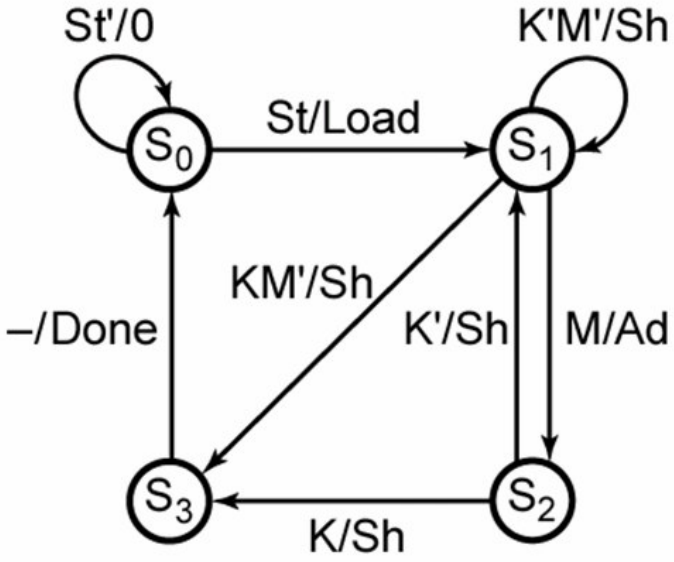


(a) Multiplier control

Figure 18-9



(b) State graph for add-shift control



(c) Final state graph for add-shift control

Table 18.2 Operation of a Multiplier Using a Counter

Time	State	Counter	Product Register	St	M	K	Load	Ad	Sh	Done
t_0	S_0	00	000000000	0	0	0	0	0	0	0
t_1	S_0	00	000000000	1	0	0	1	0	0	0
t_2	S_1	00	000001011	0	1	0	0	1	0	0
t_3	S_2	00	011011011	0	1	0	0	0	1	0
t_4	S_1	01	001101101	0	1	0	0	1	0	0
t_5	S_2	01	100111101	0	1	0	0	0	1	0
t_6	S_1	10	010011110	0	0	0	0	0	1	0
t_7	S_1	11	001001111	0	1	1	0	1	0	0
t_8	S_2	11	100011111	0	1	1	0	0	1	0
t_9	S_3	00	010001111	0	1	0	0	0	0	1

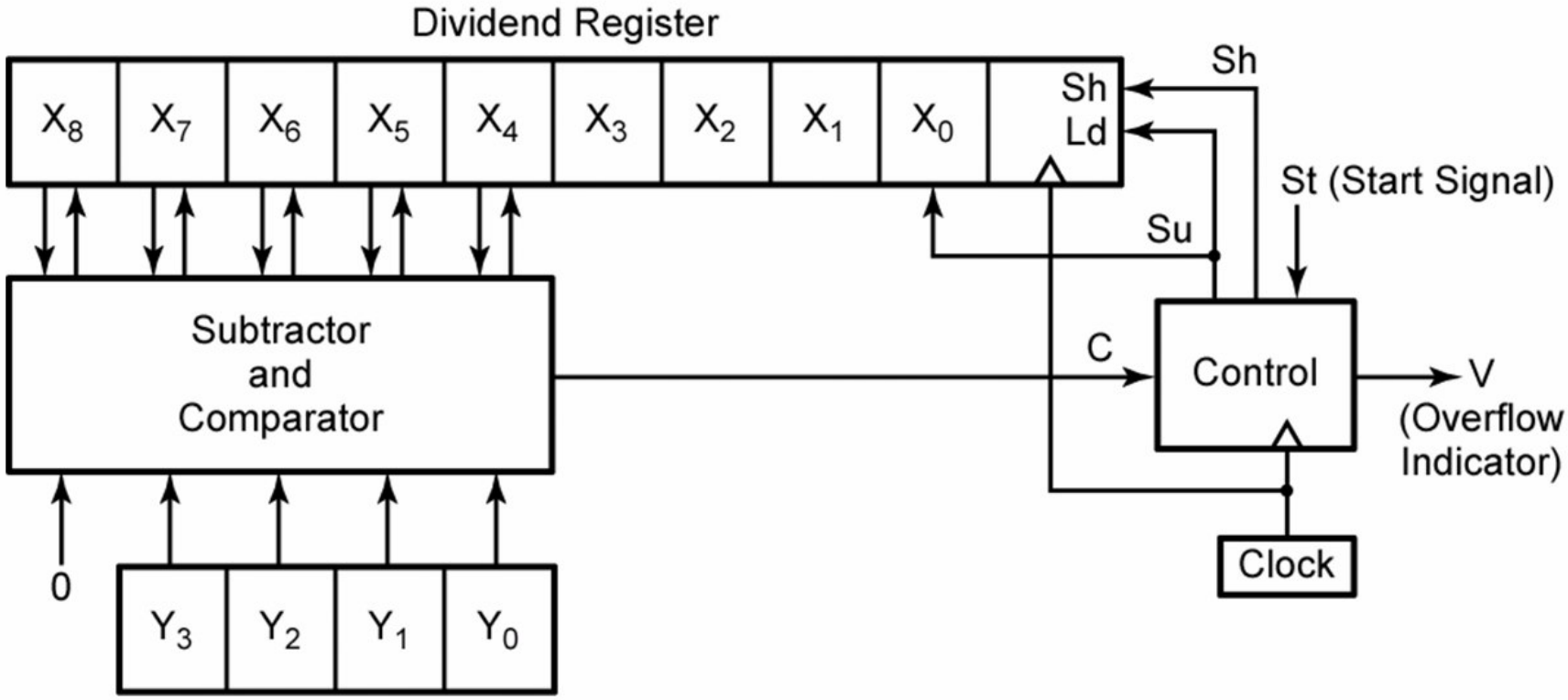


Figure 18-10: **Block Diagram for Parallel Binary Divider**

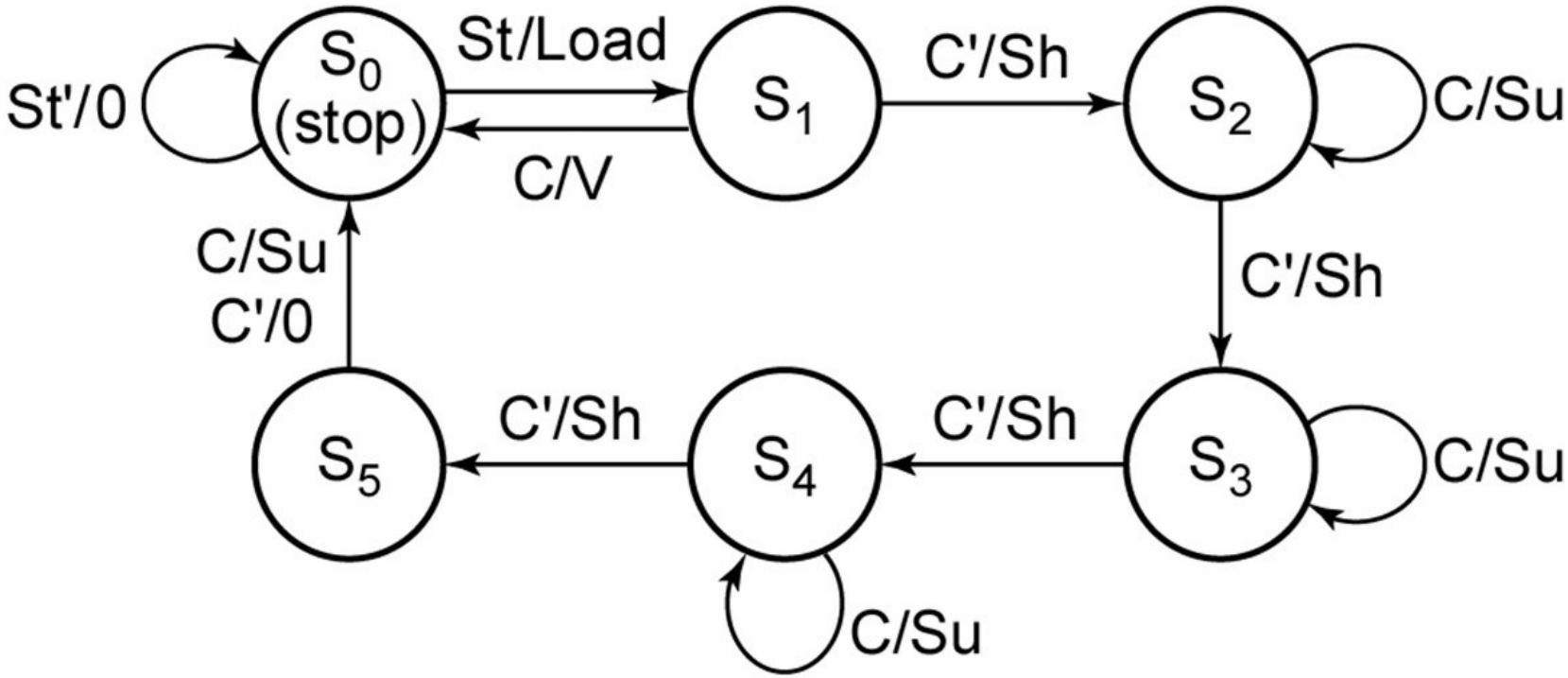


Figure 18-11: **State Graph for Divider Control Circuit**

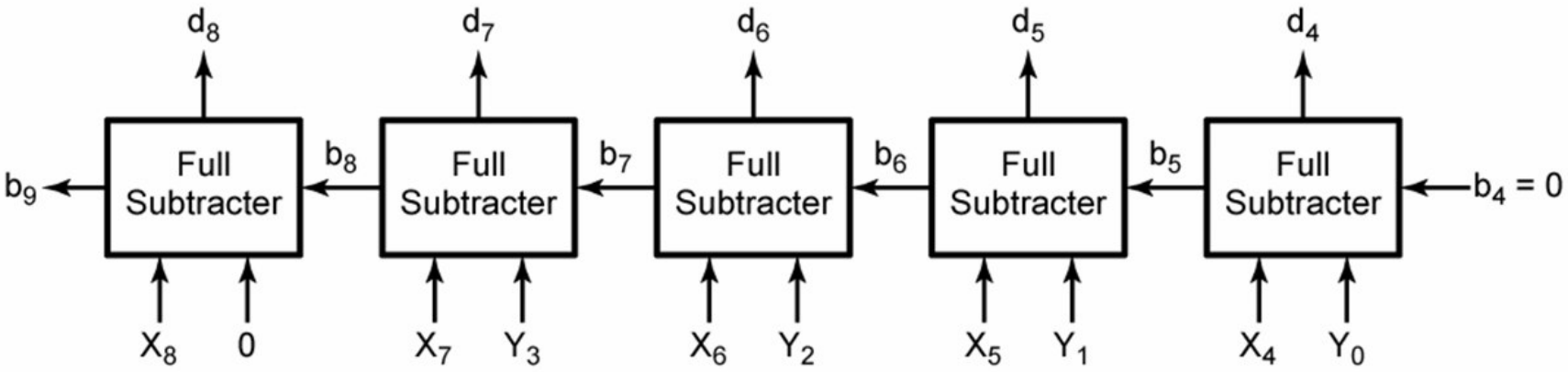
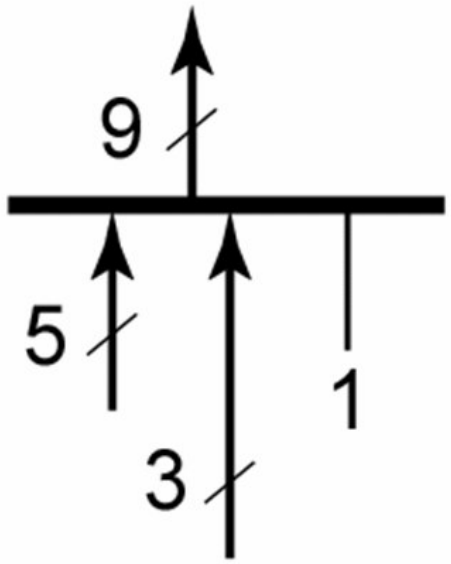
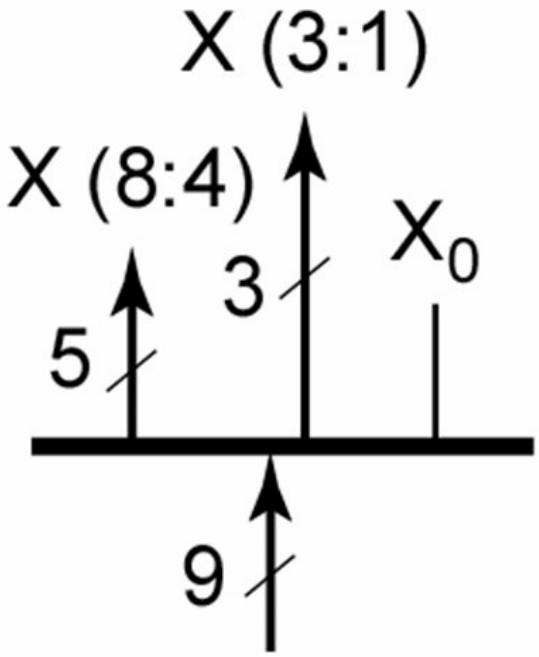


Figure 18-12: **Logic Diagram for 5-Bit Subtracter**



Bus Merger



Bus Splitter

Section 18.3, p. 550

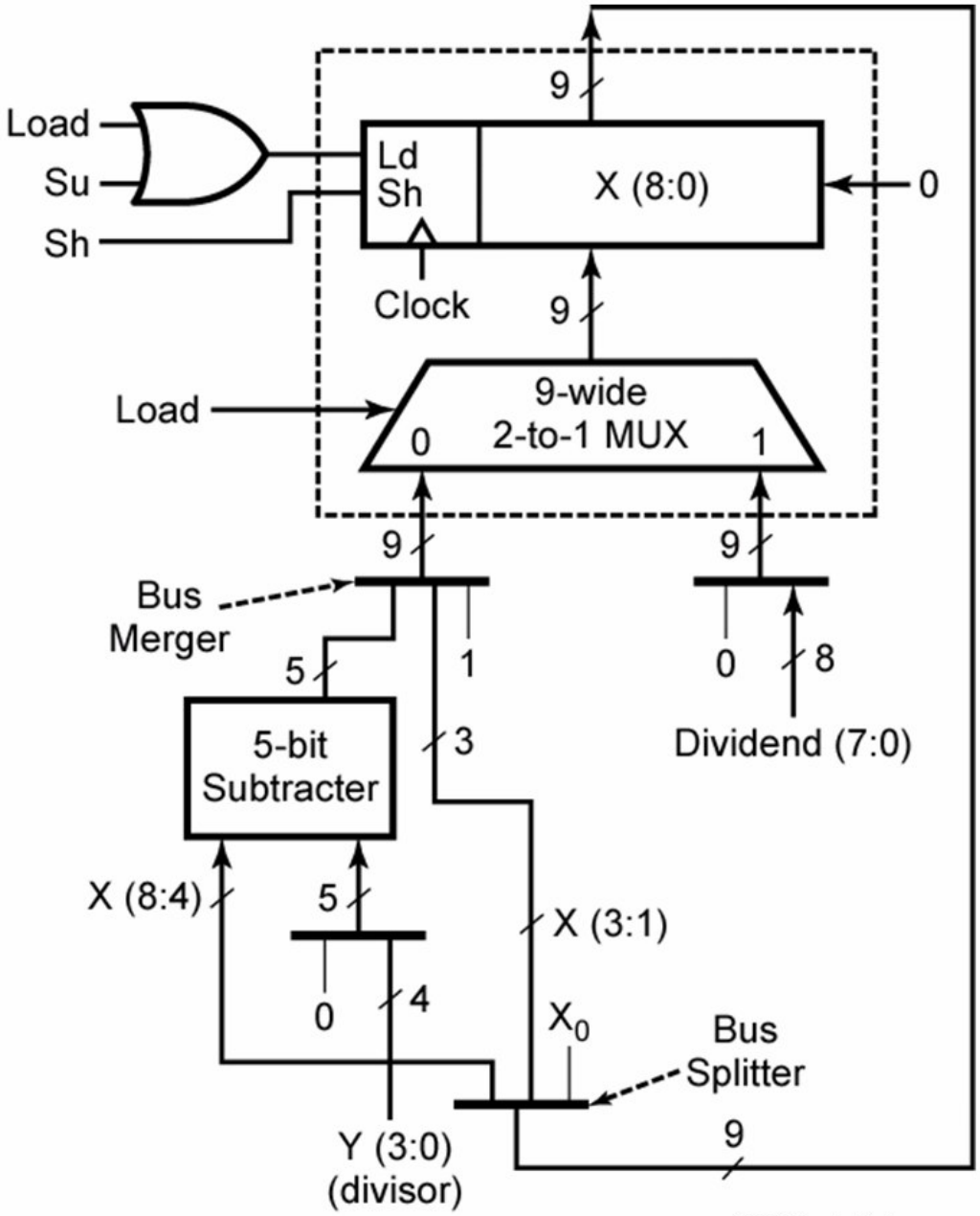


Figure 18-13:

Block Diagram for Divider Using Bus Notation