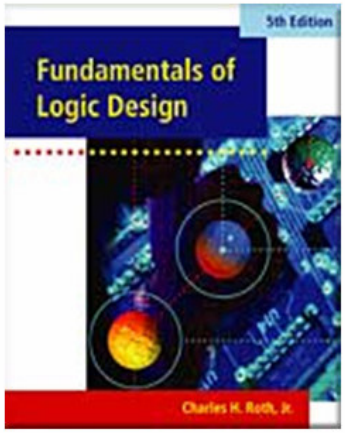
FIGURES FOR

CHAPTER 16

SEQUENTIAL CIRCUIT DESIGN



This chapter in the book includes:

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Table 16-1.

X Input (BCD)				Z Output (excess-3)			
t_3	t_2	t_1	t_0	t_3	t_2	t_1	t_0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

Table 16-2. State Table for Code Converter

Time	Input Sequence Received (Least Significant Bit First)	Present State	Next State $X=0$	Next State 1	Present Output (Z) $X=0$	Present Output (Z) 1
t_0	reset	A	B	C	1	0
t_1	0	B	D	F	1	0
	1	C	E	G	0	1
t_2	00	D	H	L	0	1
	01	E	I	M	1	0
	10	F	J	N	1	0
	11	G	K	P	1	0
t_3	000	H	A	A	0	1
	001	I	A	A	0	1
	010	J	A	–	0	–
	011	K	A	–	0	–
	100	L	A	–	0	–
	101	M	A	–	1	–
	110	N	A	–	1	–
	111	P	A	–	1	–

Table 16-3. Reduced State Table for Code Converter

Time	Present State	Next State $X = 0$	Next State 1	Present Output (Z) $X = 0$	Present Output (Z) 1
t_0	A	B	C	1	0
t_1	B	D	E	1	0
	C	E	E	0	1
t_2	D	H	H	0	1
	E	H	M	1	0
t_3	H	A	A	0	1
	M	A	–	1	–

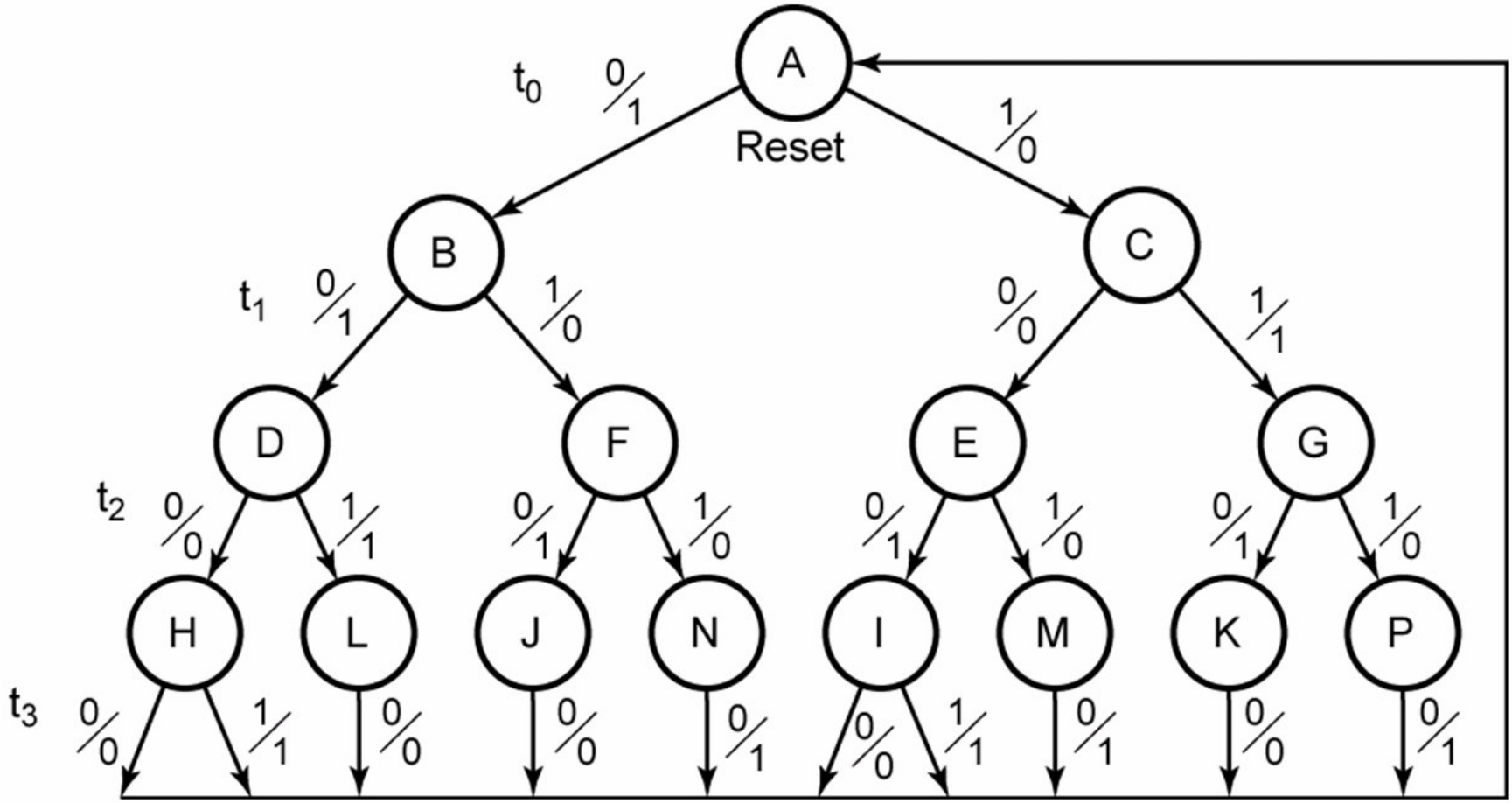
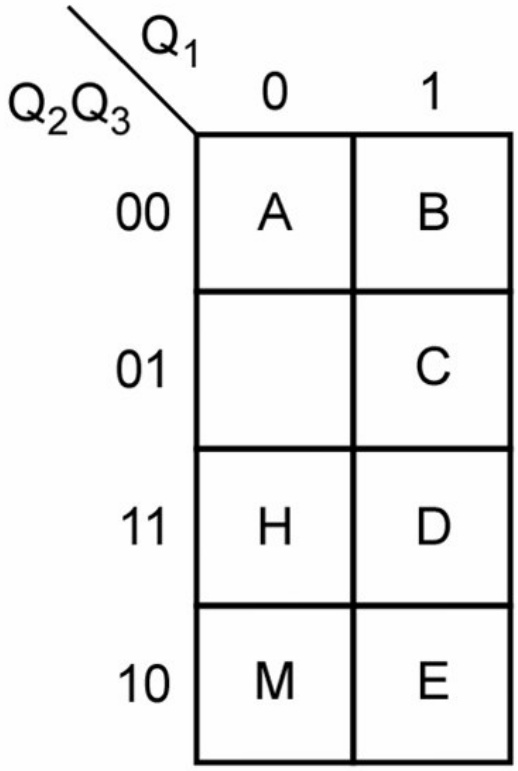


Figure 16-1: **State Graph for Code Converter**



(a) Assignment map

	$Q_1Q_2Q_3$	$Q_1^+Q_2^+Q_3^+$		Z	
		$X = 0$	$X = 1$	$X = 0$	$X = 1$
A	000	100	101	1	0
B	100	111	110	1	0
C	101	110	110	0	1
D	111	011	011	0	1
E	110	011	010	1	0
H	011	000	000	0	1
M	010	000	xxx	1	x
-	001	xxx	xxx	x	x

(b) Transition table

Figure 16-2: **Assignment Map for Flip Flops**

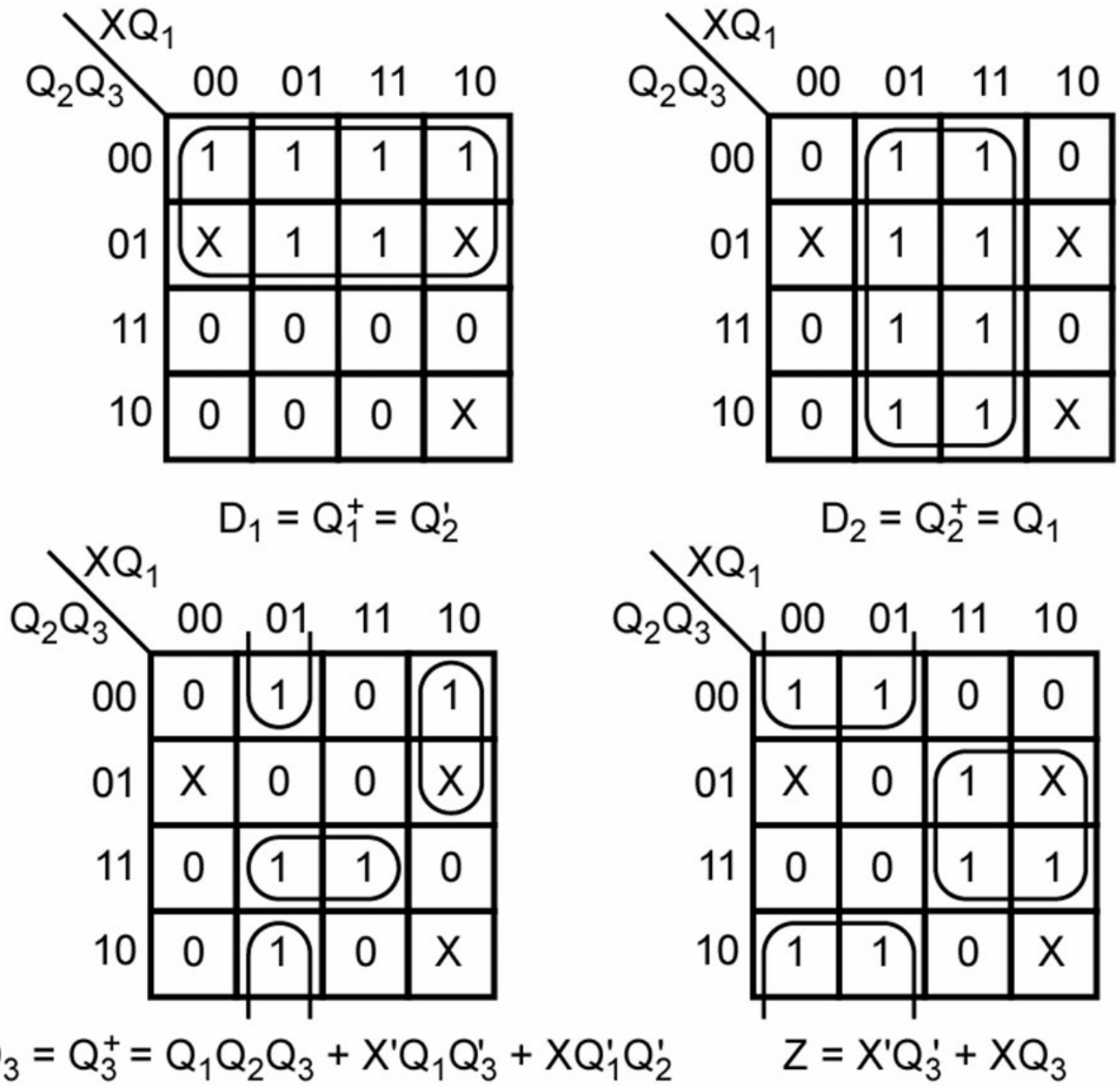


Figure 16-3: **Karnaugh Maps for Code Converter Design**

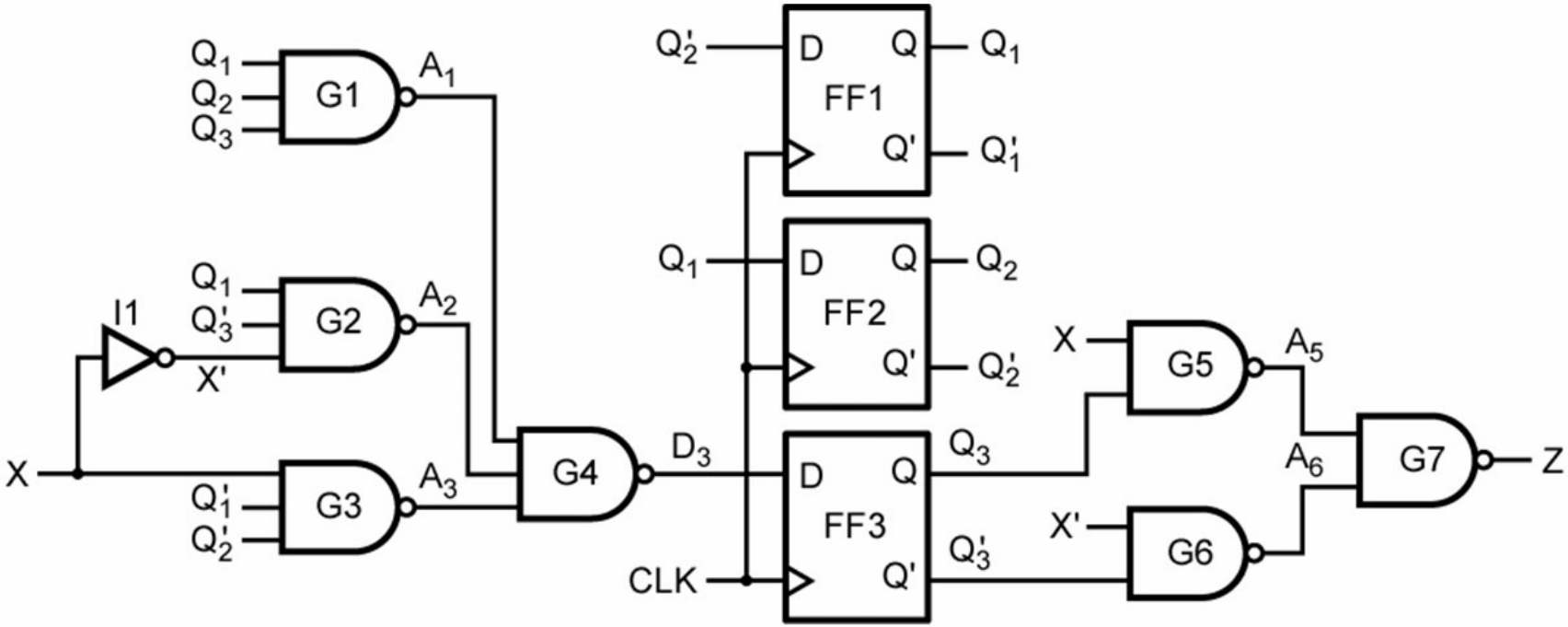


Figure 16-4: **Code Converter Circuit**

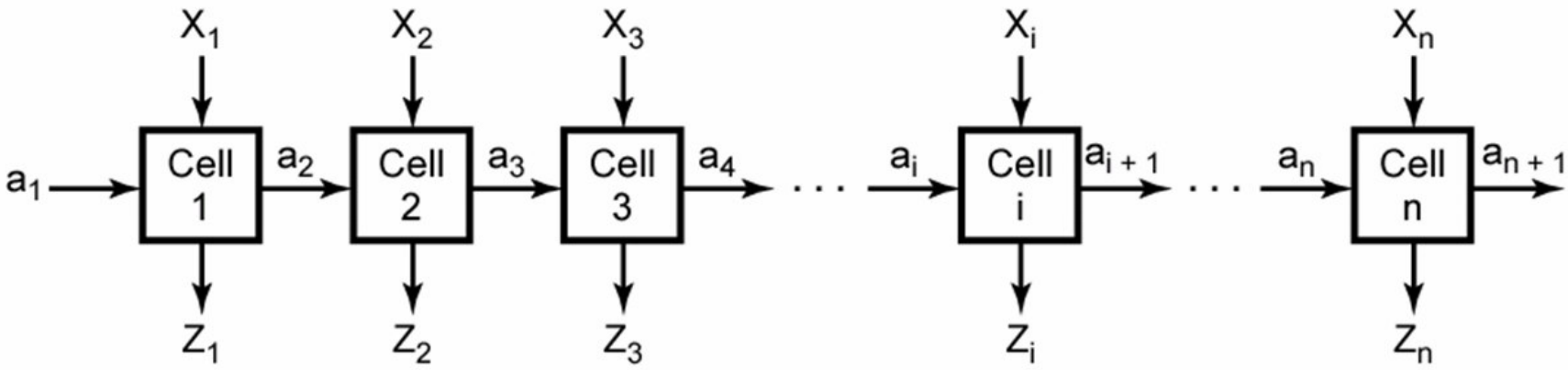


Figure 16-5: **Unilateral Iterative Circuit**

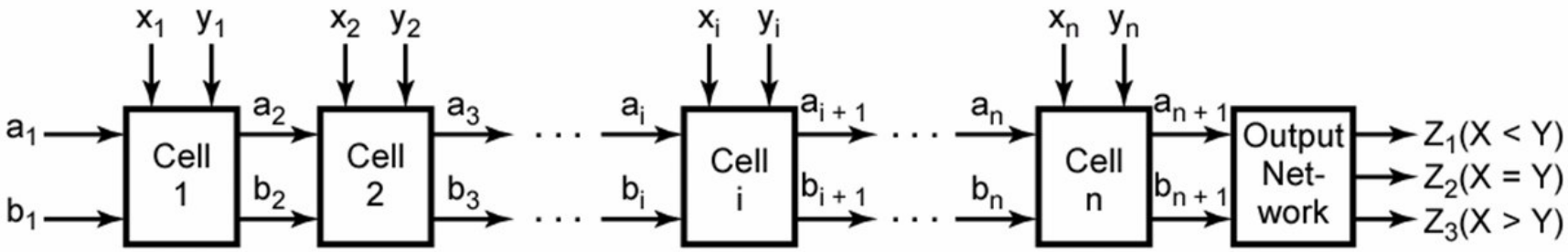


Figure 16-6: **Form of Iterative Circuit for Comparing Binary Numbers**

Table 16-4 State Table for Comparator

		S_{i+1}				
	S_i	$x_iy_i = 00$	01	11	10	$Z_1Z_2Z_3$
$X = Y$	S_0	S_0	S_2	S_0	S_1	0 1 0
$X > Y$	S_1	S_1	S_1	S_1	S_1	0 0 1
$X < Y$	S_2	S_2	S_2	S_2	S_2	1 0 0

Table 16-5 Transition Table for Comparator

a_ib_i	$a_{i+1}b_{i+1}$ $x_iy_i = 00$	01	11	10	$Z_1Z_2Z_3$
0 0	00	10	00	01	0 1 0
0 1	01	01	01	01	0 0 1
1 0	10	10	10	10	1 0 0

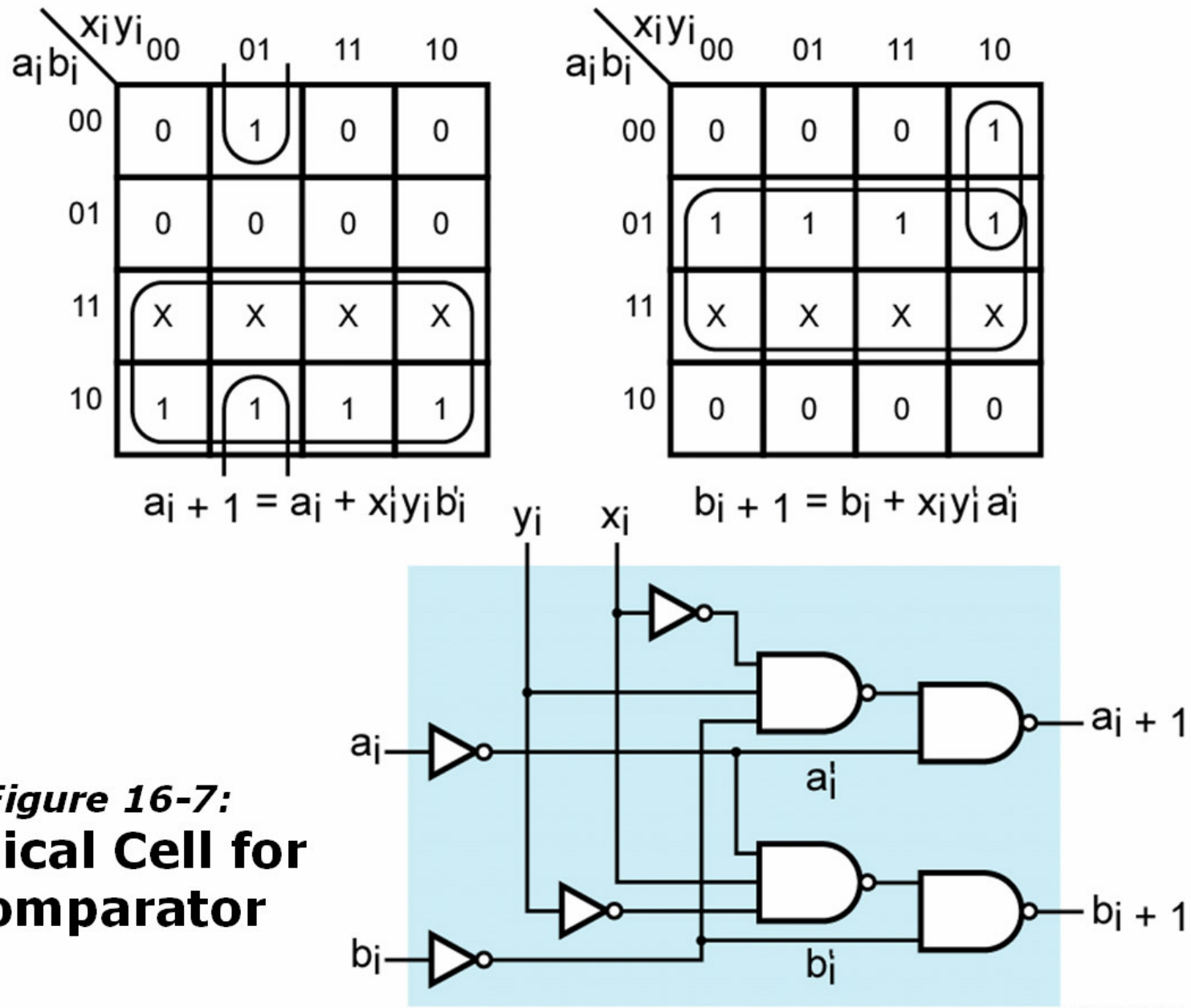


Figure 16-7:
Typical Cell for Comparator

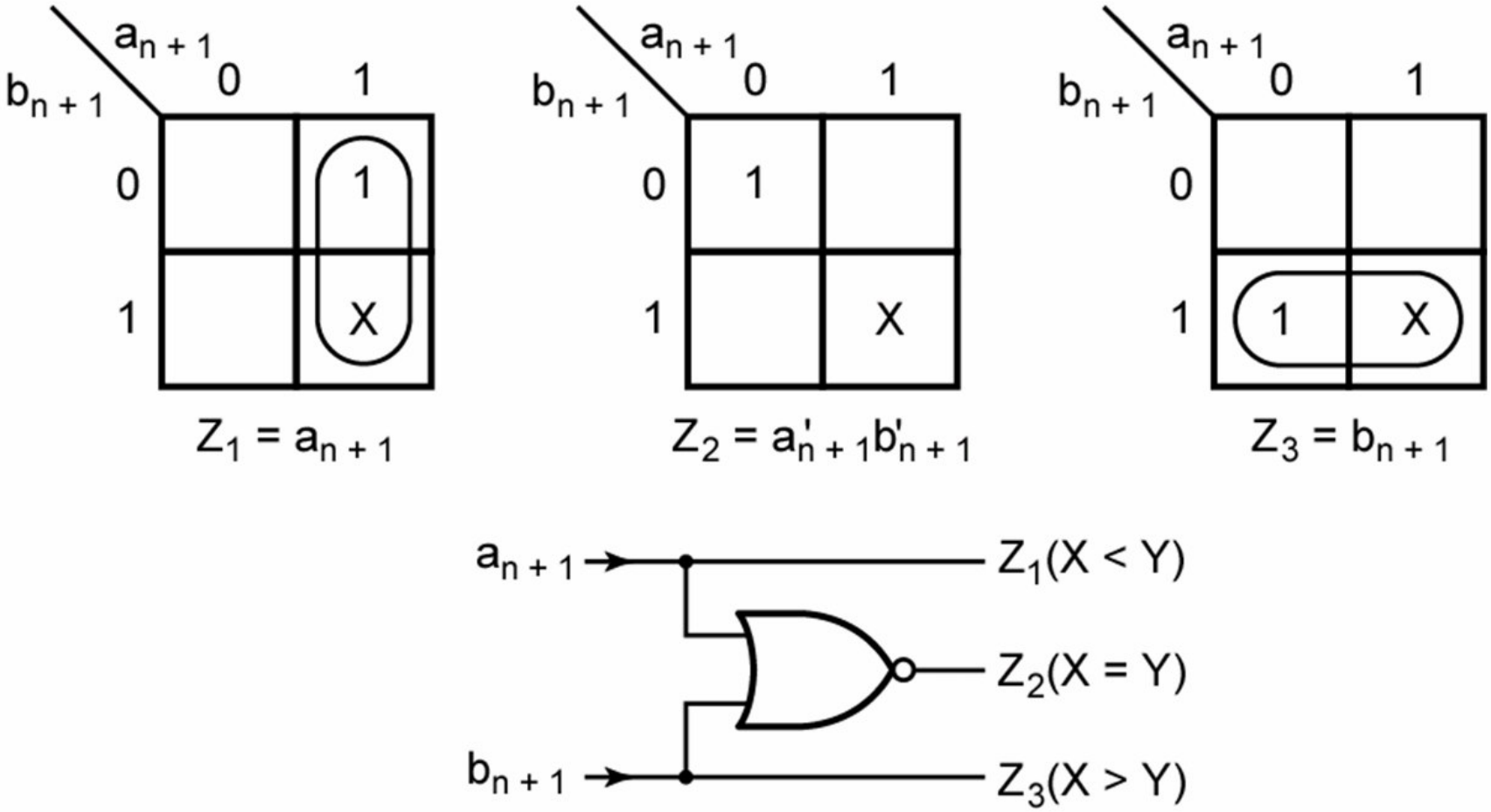


Figure 16-8: **Output Circuit for Comparator**

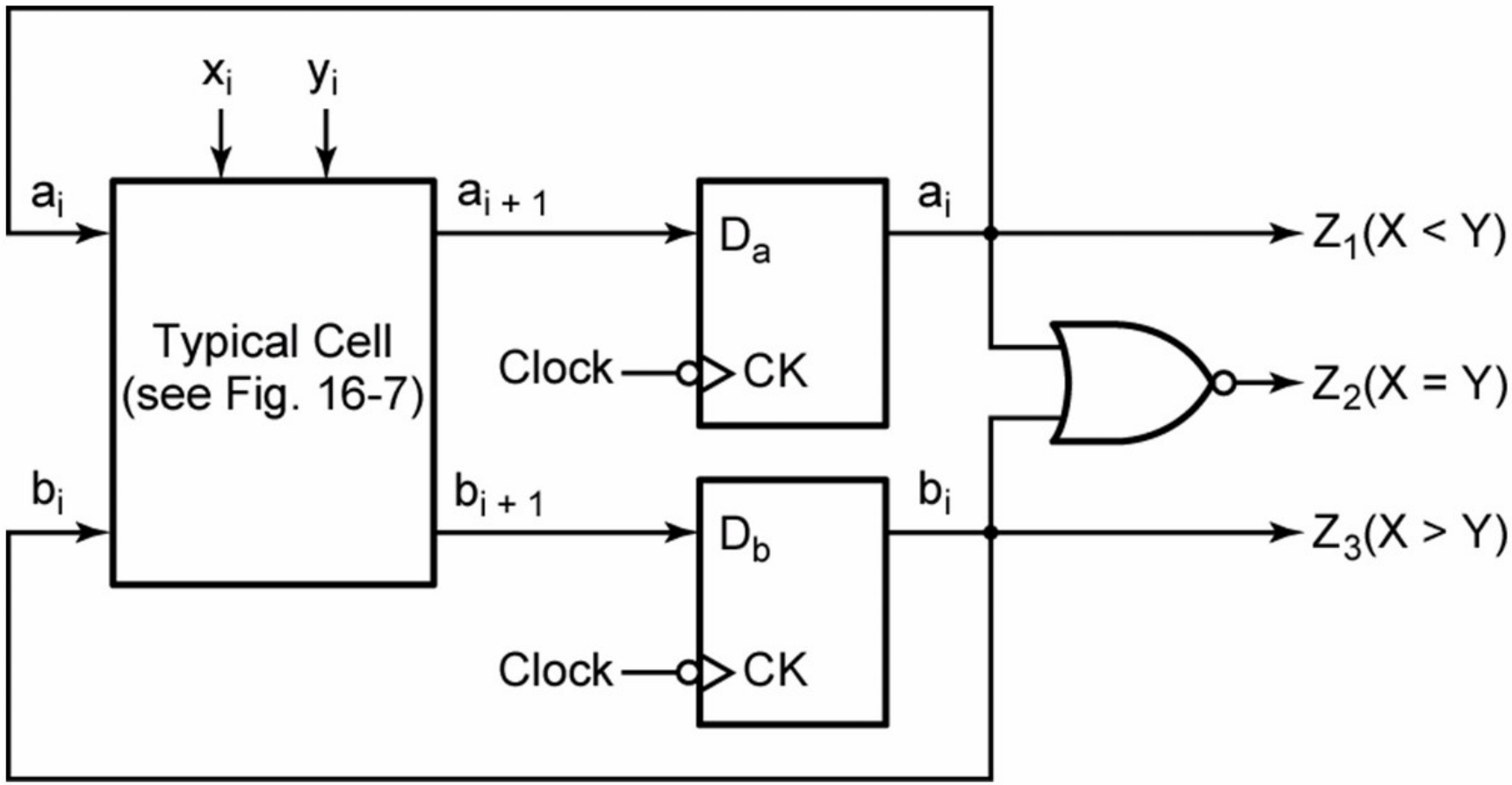


Figure 16-9: **Sequential Comparator for Binary Numbers**

Table 16-6a

(a) state table

Present State	Next State $X=0$	Next State 1	Present Output (Z) $X=0$	Present Output (Z) 1
A	B	C	1	0
B	D	E	1	0
C	E	E	0	1
D	H	H	0	1
E	H	M	1	0
H	A	A	0	1
M	A	–	1	–

Table 16-6b

(b) transition table

	$Q_1Q_2Q_3$	$Q_1^+Q_2^+Q_3^+$		Z	
		$X = 0$	$X = 1$	$X = 0$	$X = 1$
A	000	001	010	1	0
B	001	011	100	1	0
C	010	100	100	0	1
D	011	101	101	0	1
E	100	101	110	1	0
H	101	000	000	0	1
M	110	000	–	1	–

Table 16-6c Truth Table

X	Q_1	Q_2	Q_3	Z	D_1	D_2	D_3
0	0	0	0	1	0	0	1
0	0	0	1	1	0	1	1
0	0	1	0	0	1	0	0
0	0	1	1	0	1	0	1
0	1	0	0	1	1	0	1
0	1	0	1	0	0	0	0
0	1	1	0	1	0	0	0
0	1	1	1	X	X	X	X
1	0	0	0	0	0	1	0
1	0	0	1	0	1	0	0
1	0	1	0	1	1	0	0
1	0	1	1	1	1	0	1
1	1	0	0	0	1	1	0
1	1	0	1	1	0	0	0
1	1	1	0	X	X	X	X
1	1	1	1	X	X	X	X

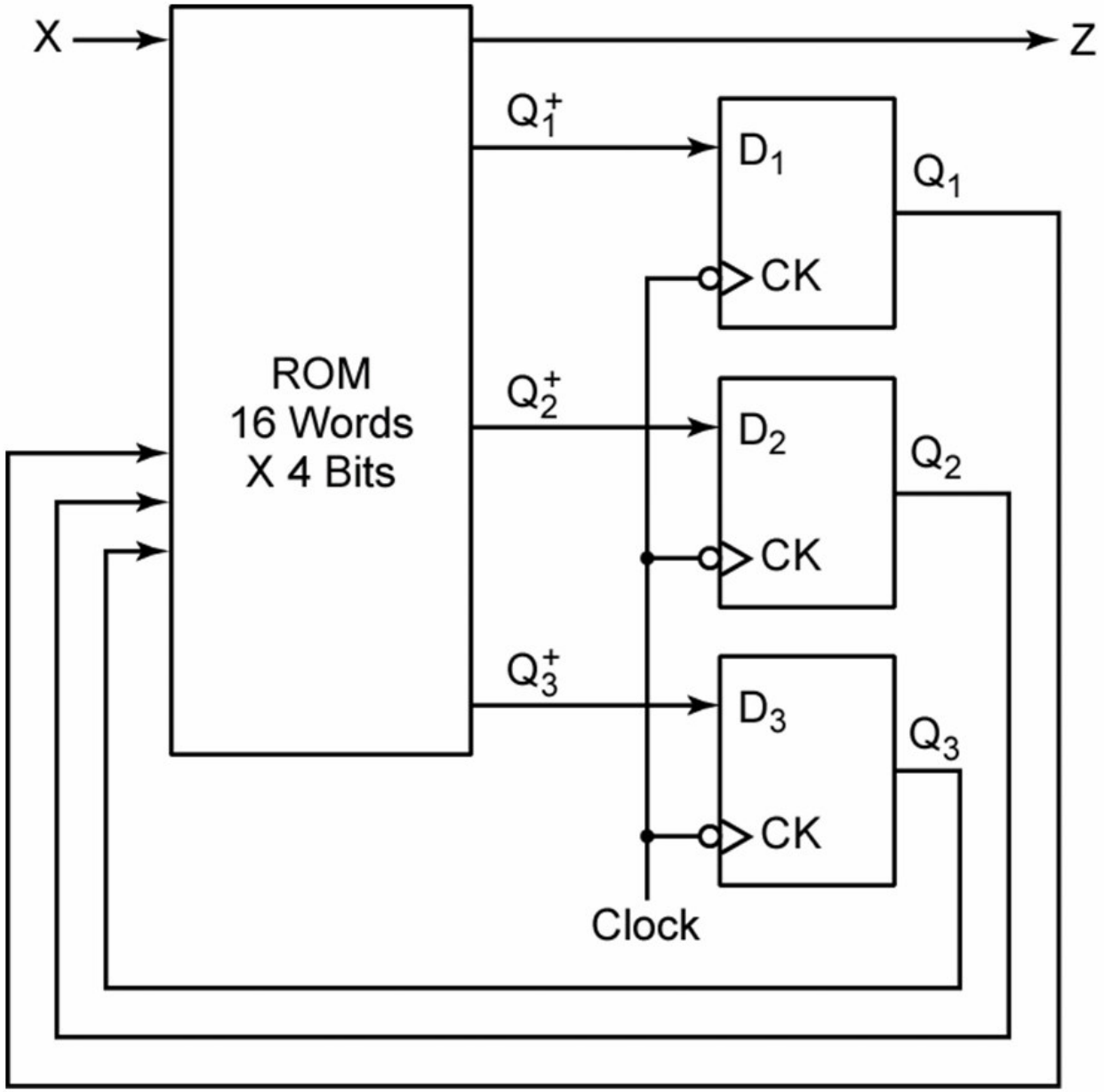


Figure 16-10:
Realization of Table 16.6(a) Using a ROM

Table 16-7

X	Q_1	Q_2	Q_3	Z	D_1	D_2	D_3
–	–	0	–	0	1	0	0
–	1	–	–	0	0	1	0
–	1	1	1	0	0	0	1
0	1	–	0	0	0	0	1
1	0	0	–	0	0	0	1
0	–	–	0	1	0	0	0
1	–	–	1	1	0	0	0

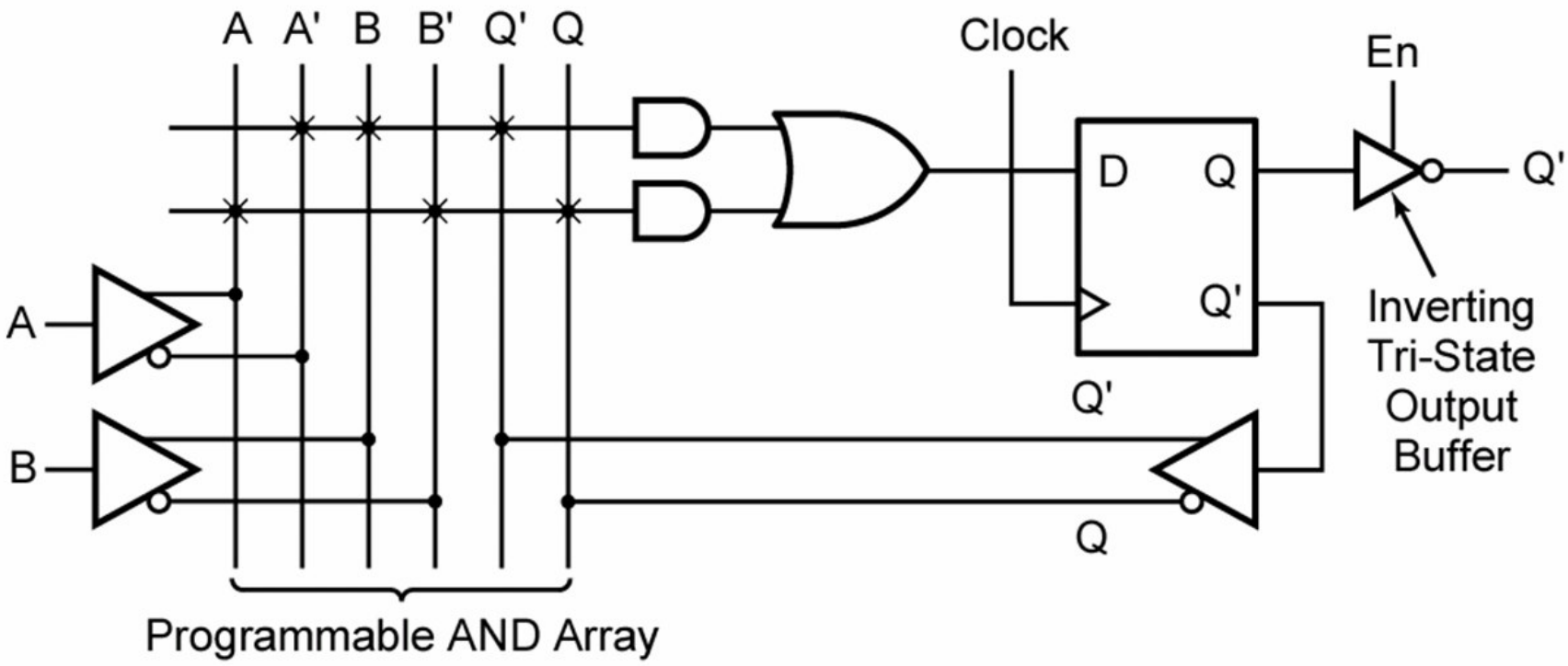


Figure 16-11: **Segment of Sequential PAL**

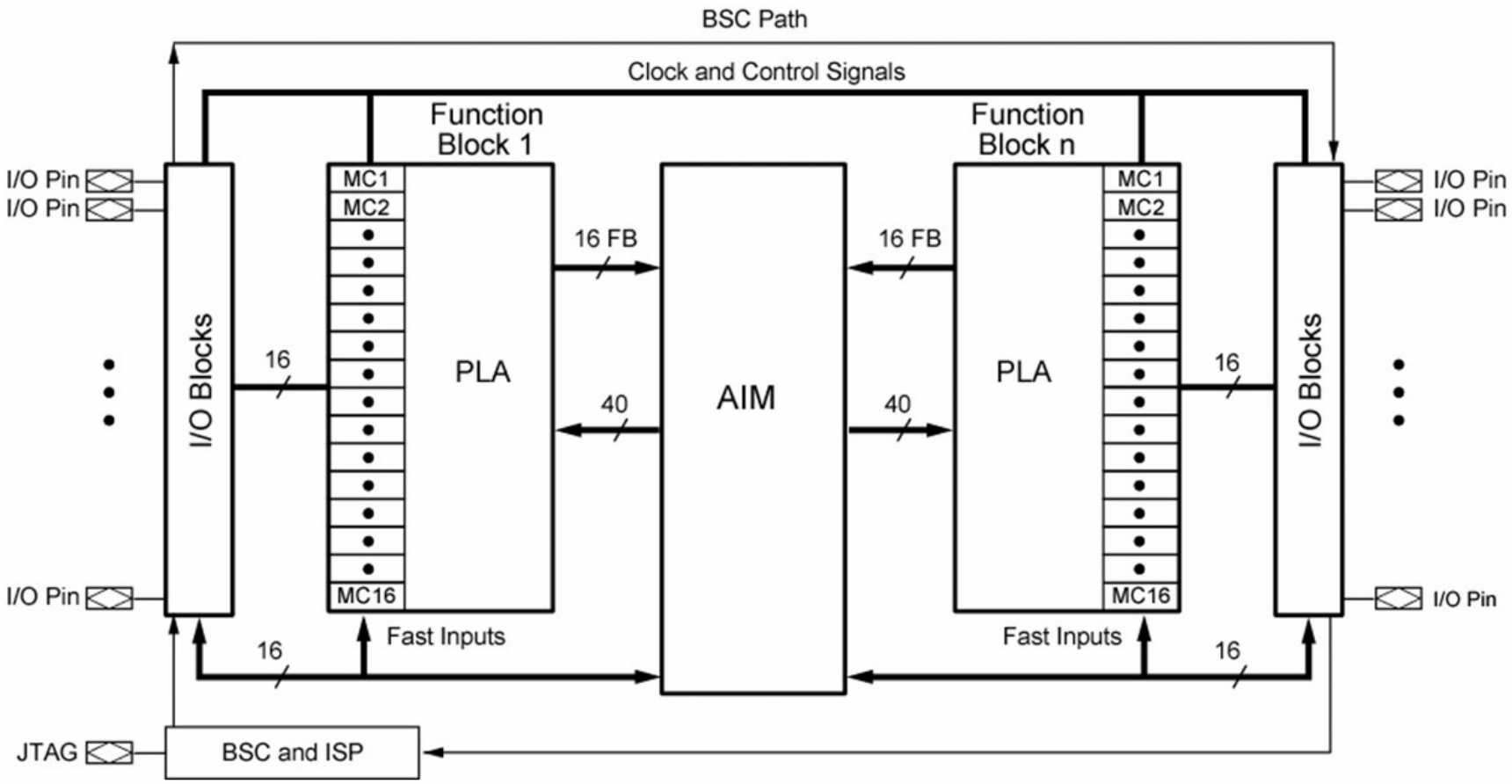


Figure 16-12: CoolRunner-II Architecture

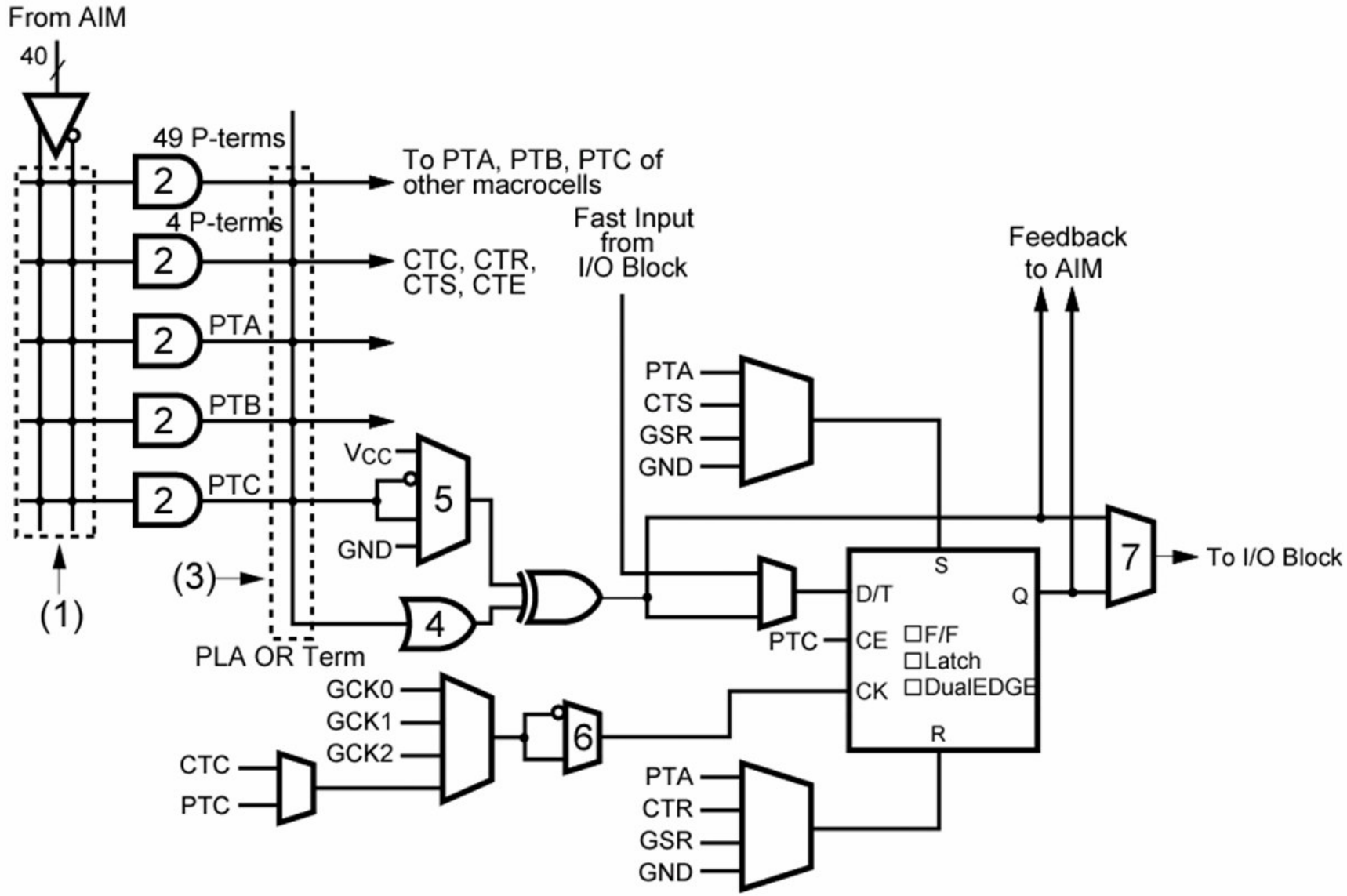


Figure 16-13: **CoolRunner-II Macrocell**

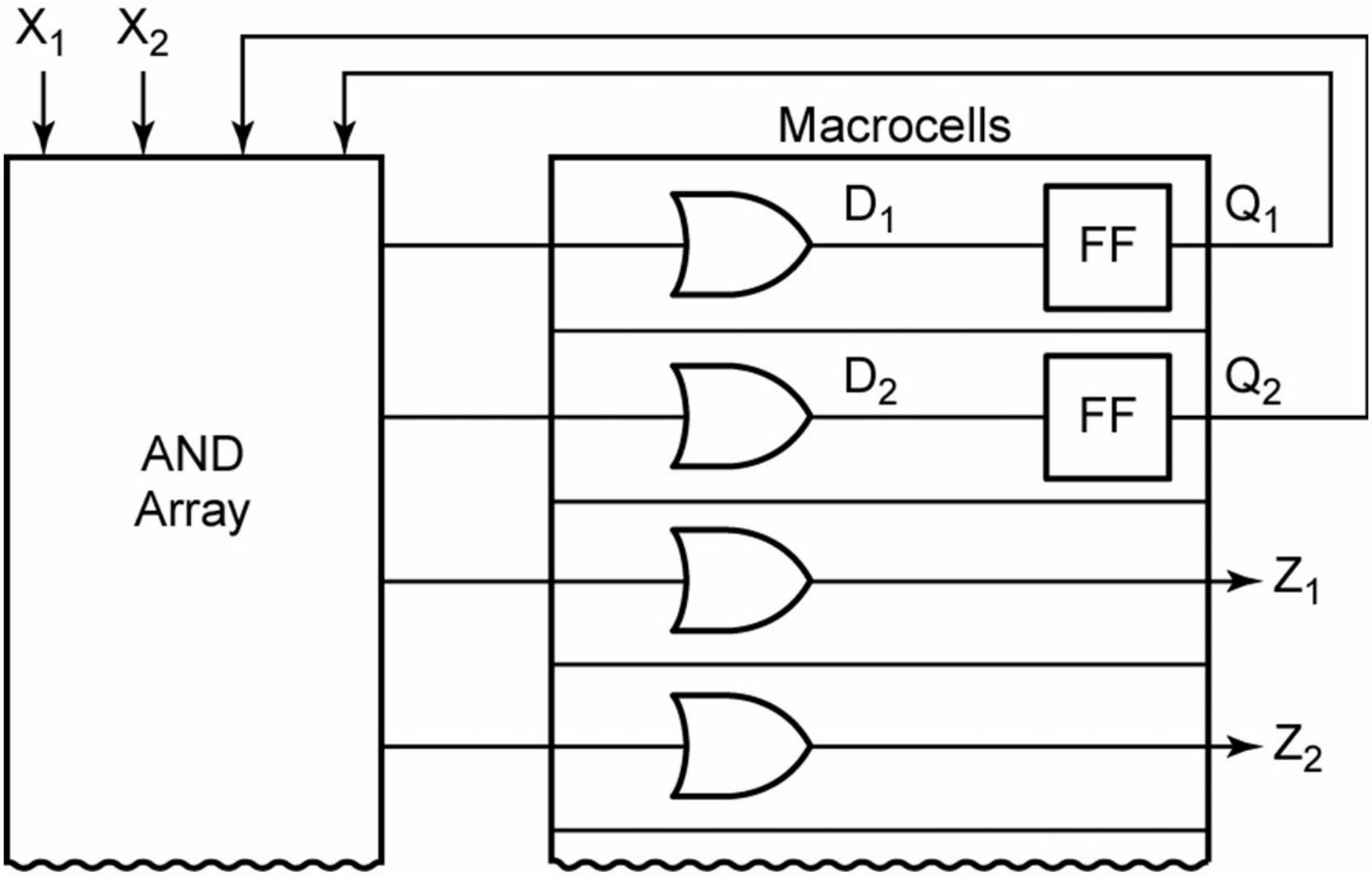


Figure 16-14: **CPLD Implementation of a Mealy Machine**

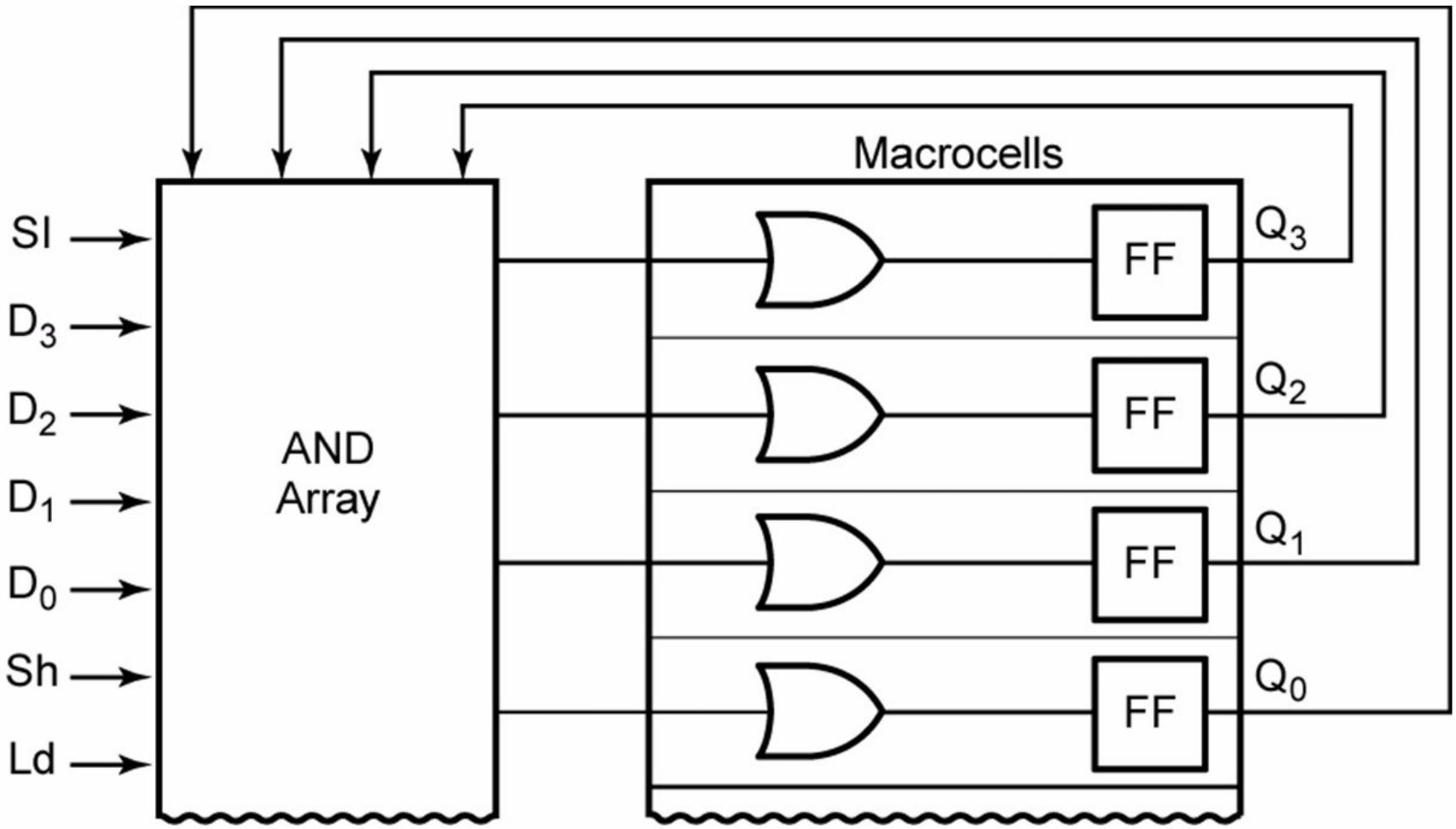


Figure 16-15: **CPLD Implementation of a Shift Register**

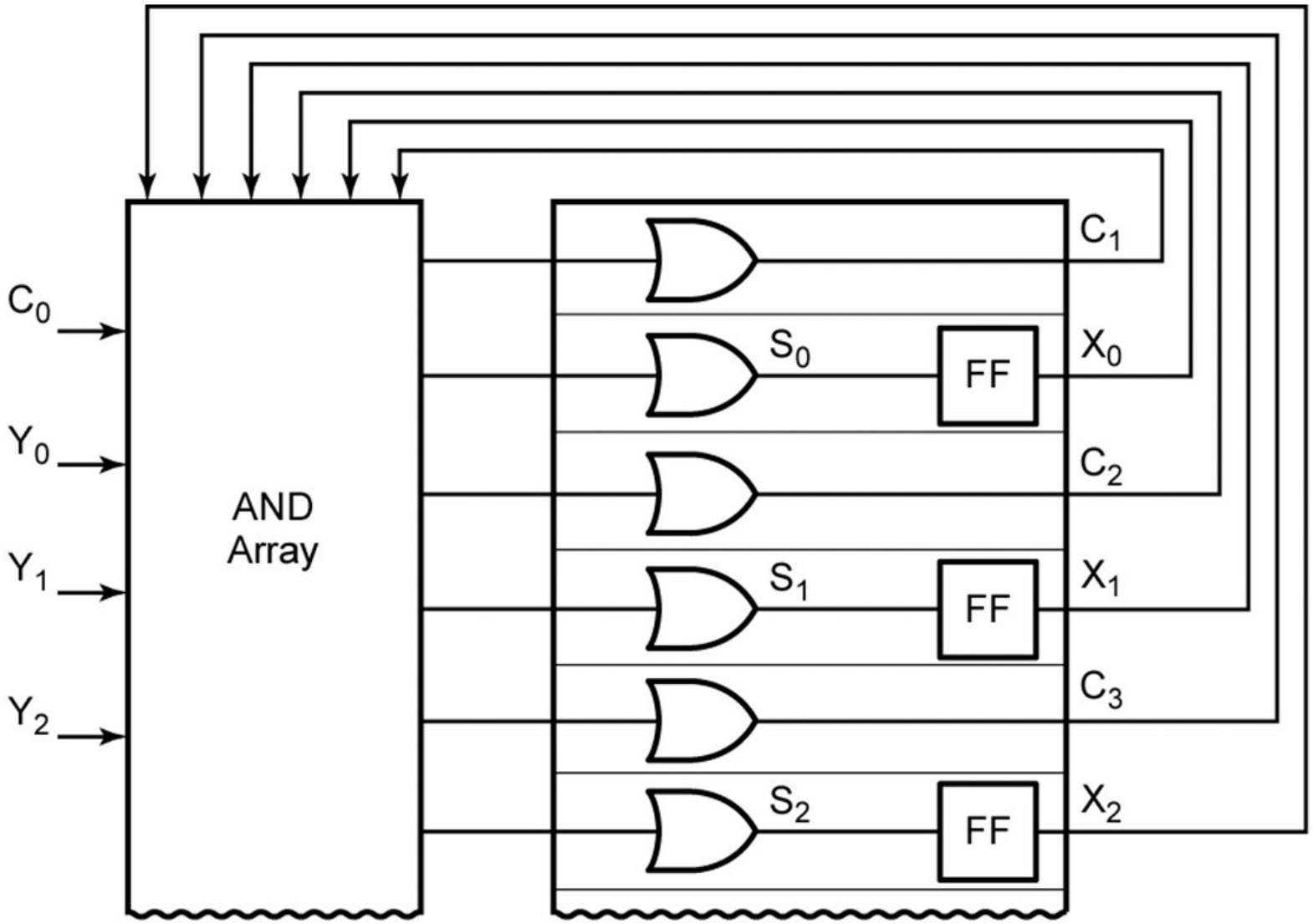


Figure 16-16: **CPLD Implementation of a Parallel Adder with Accumulator**

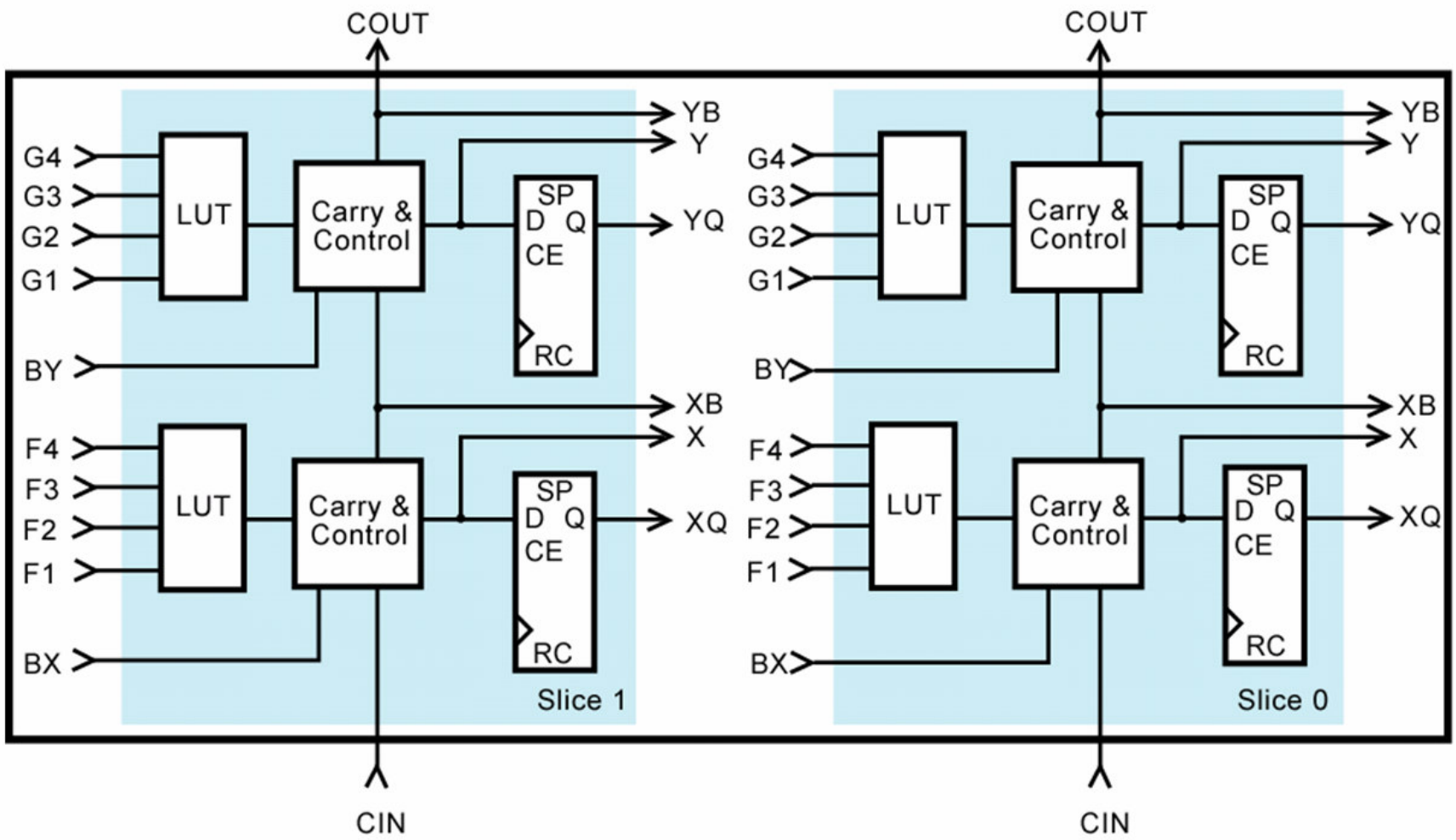


Figure 16-17: **Xilinx Virtex/Spartan II CLB** **(Figure based on figures and text owned by Xilinx, Inc., Courtesy of Xilinx, Inc. © Xilinx, Inc. 1999-2003. All rights reserved.)**

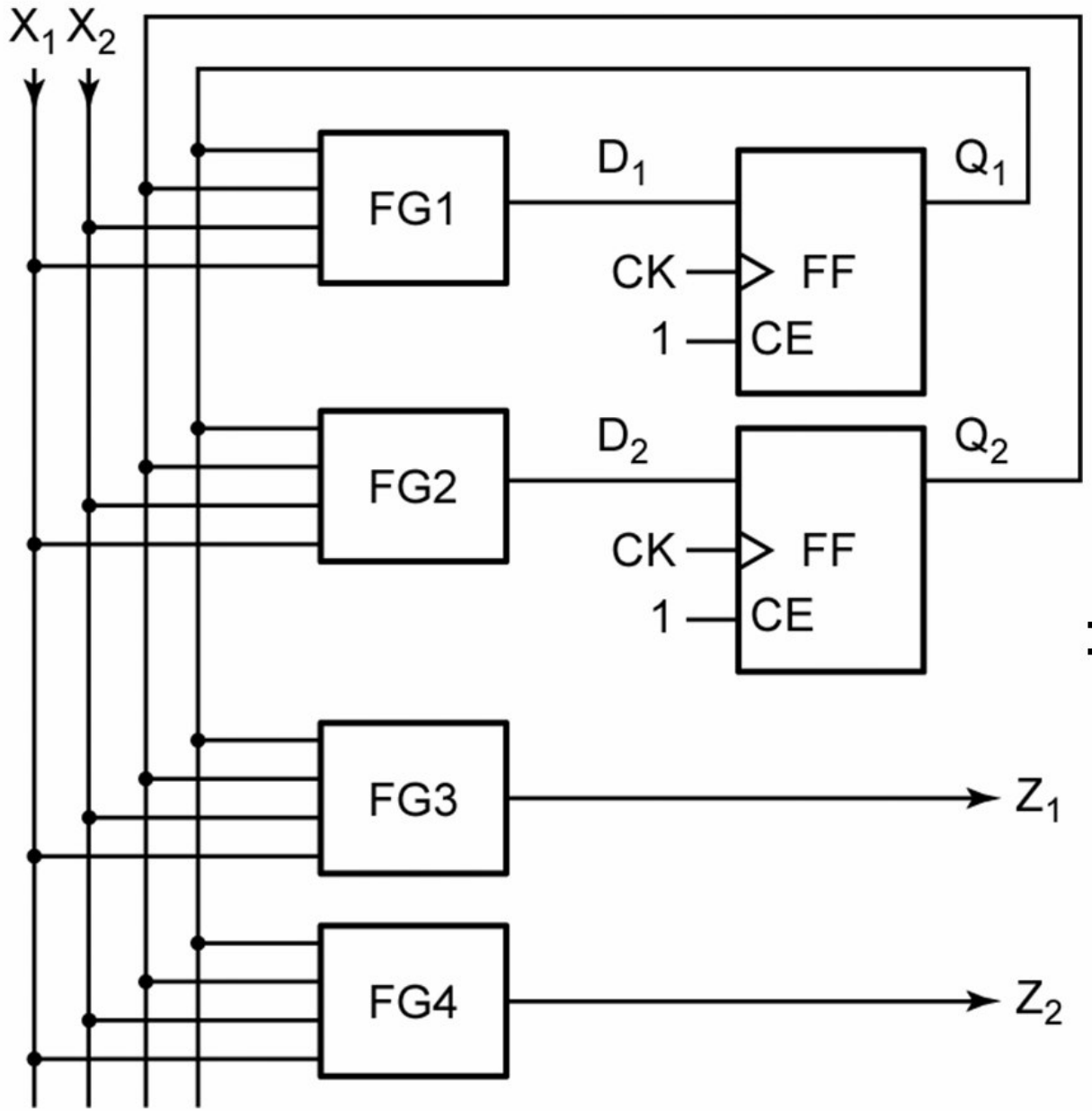


Figure 16-18:
FPGA Implementation of a Mealy Machine

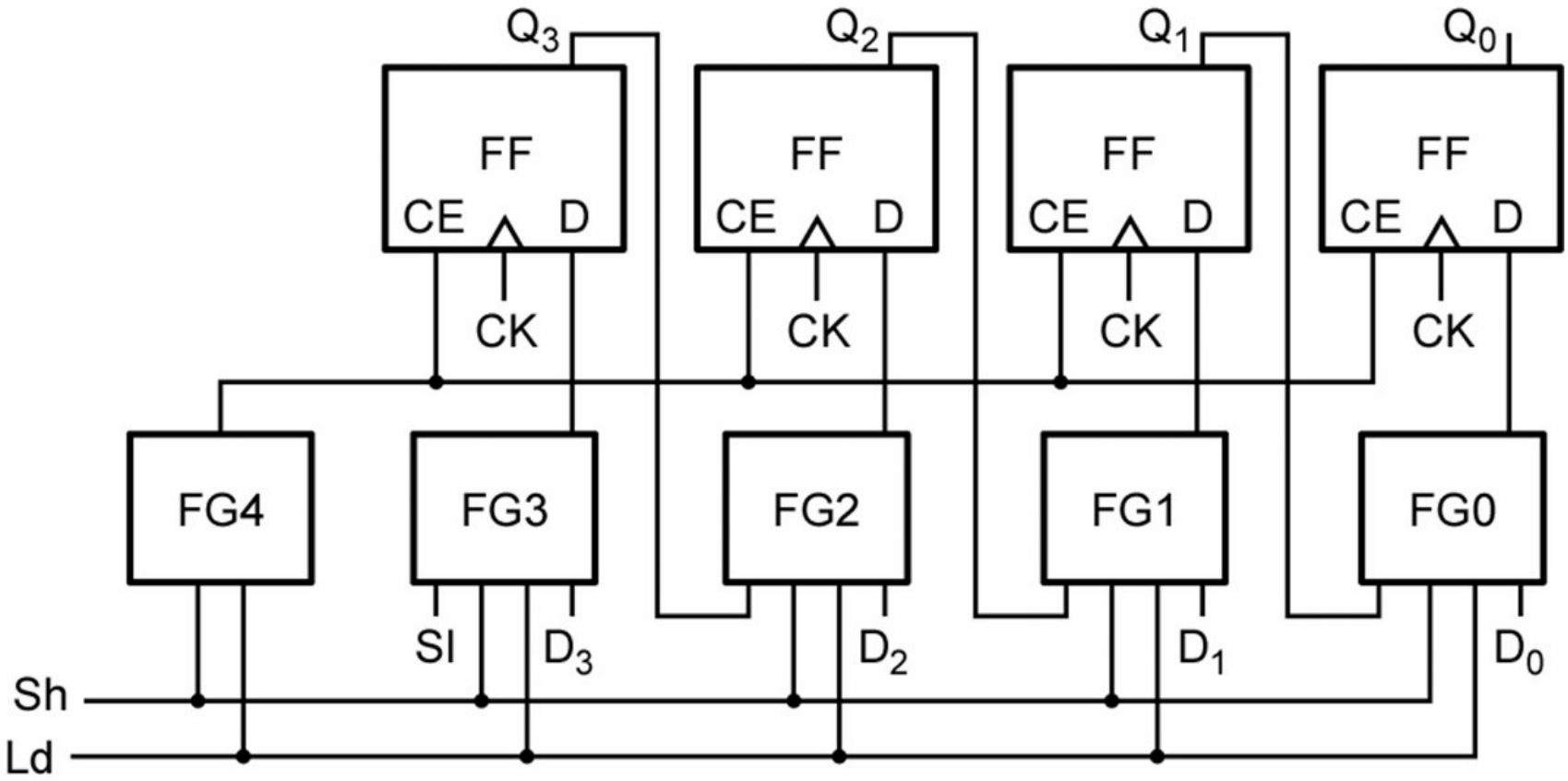


Figure 16-19: **FPGA Implementation of a Shift Register**

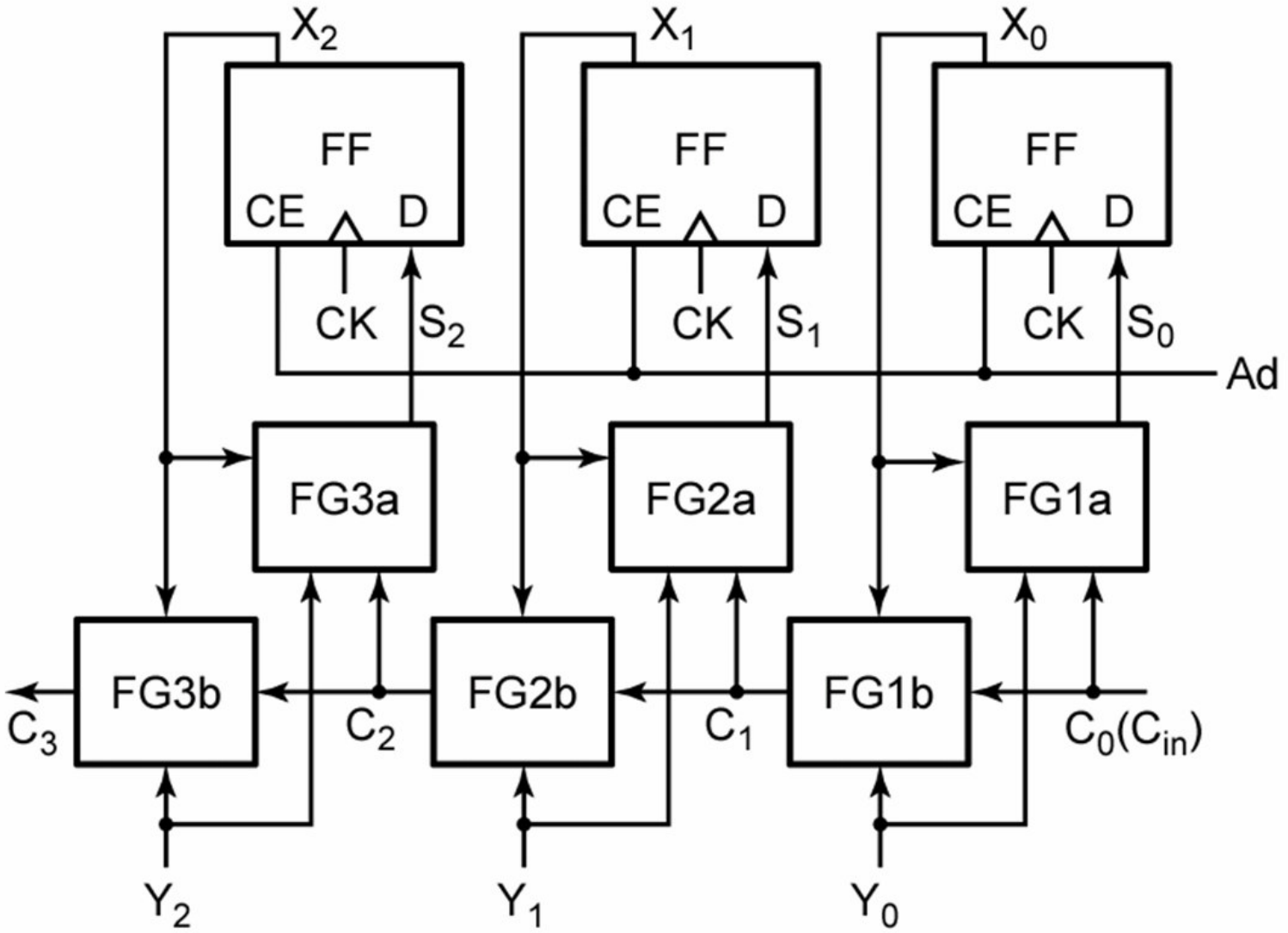


Figure 16-20: **FPGA Implementation of a Parallel Adder with Accumulator**

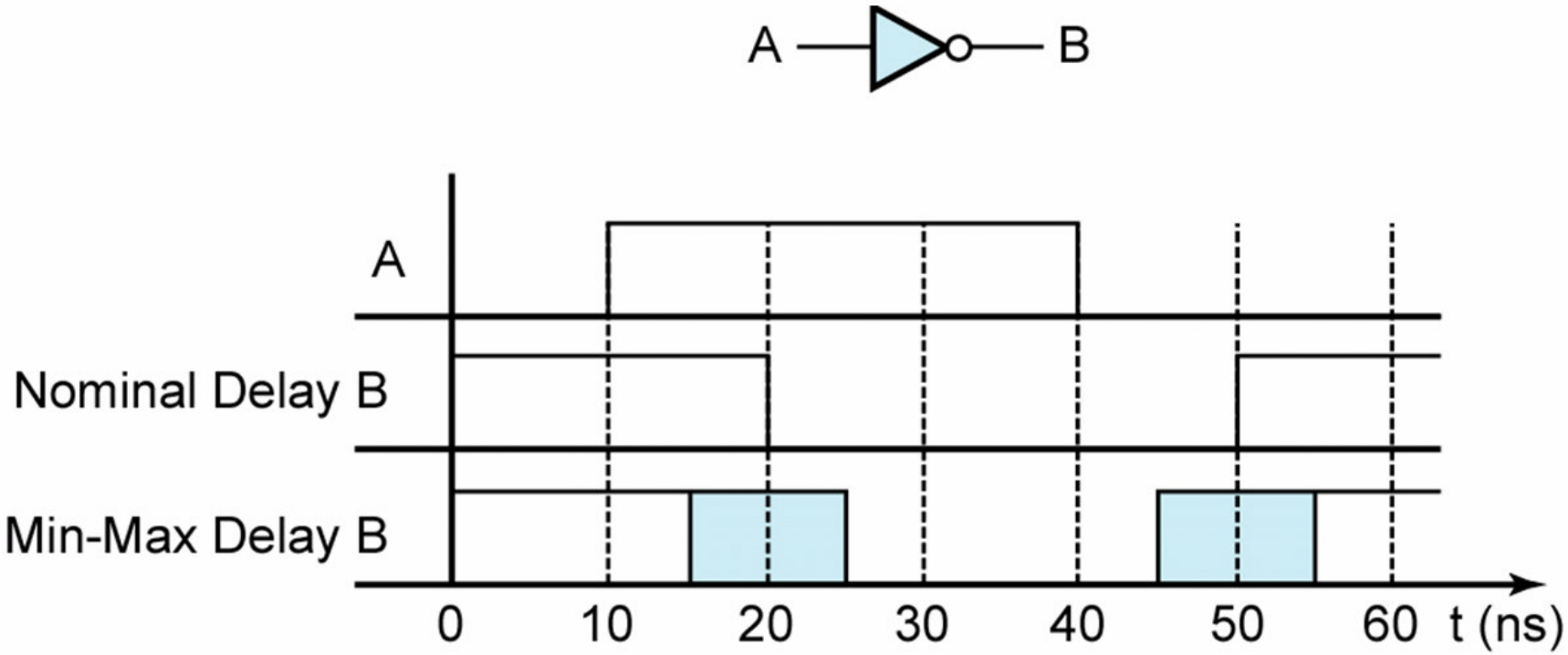


Figure 16-21: **Simulator Output for an Inverter**

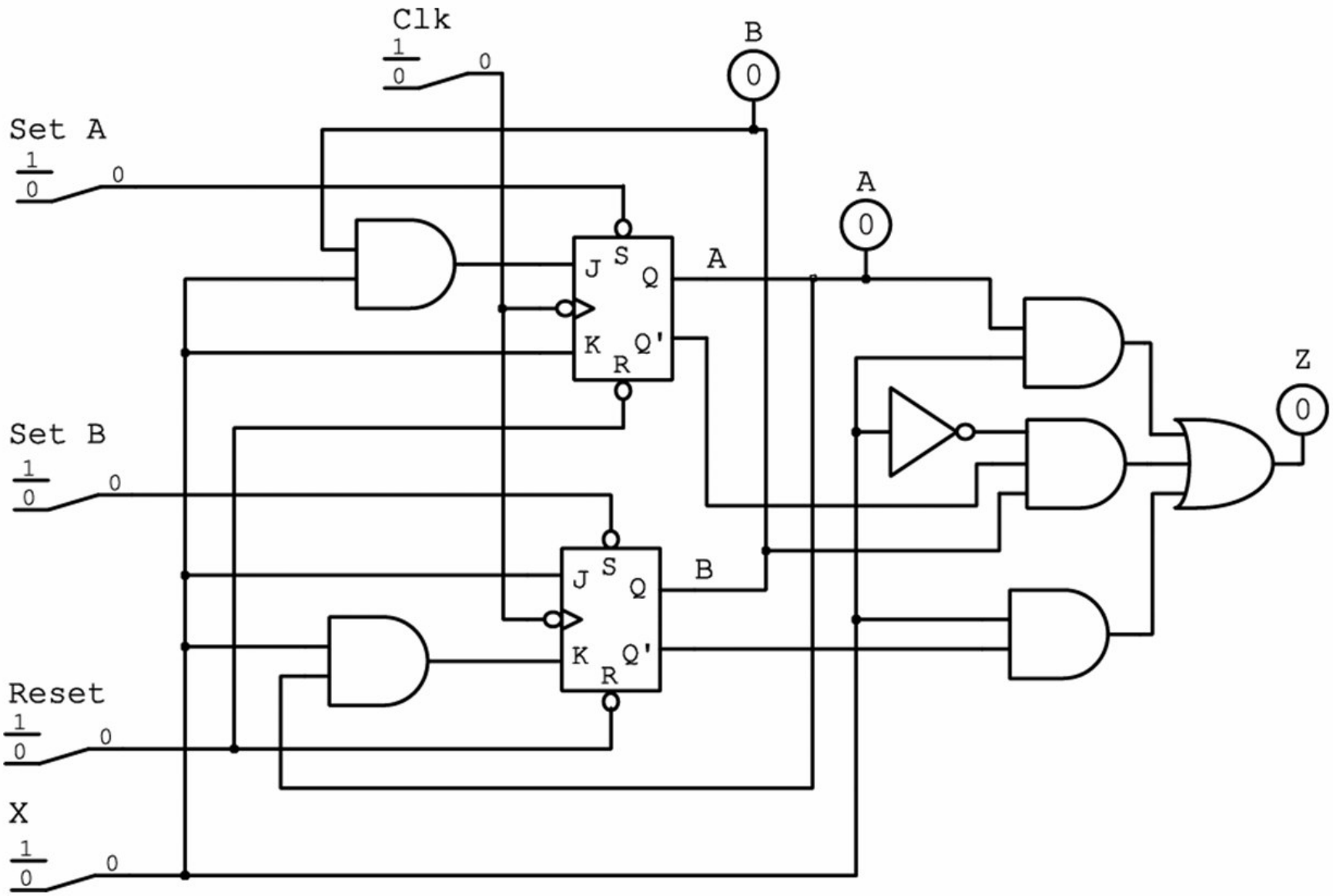
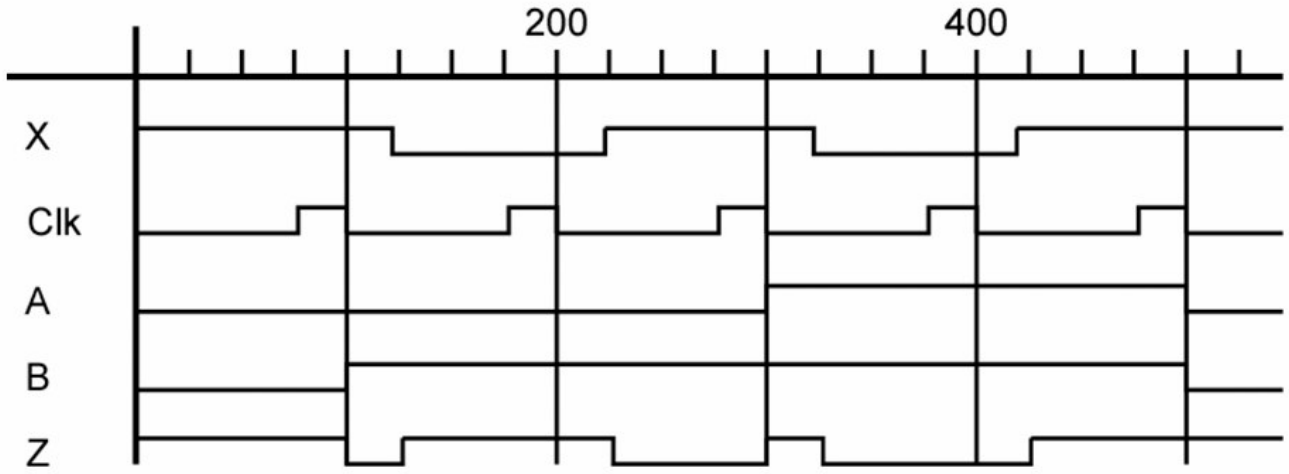
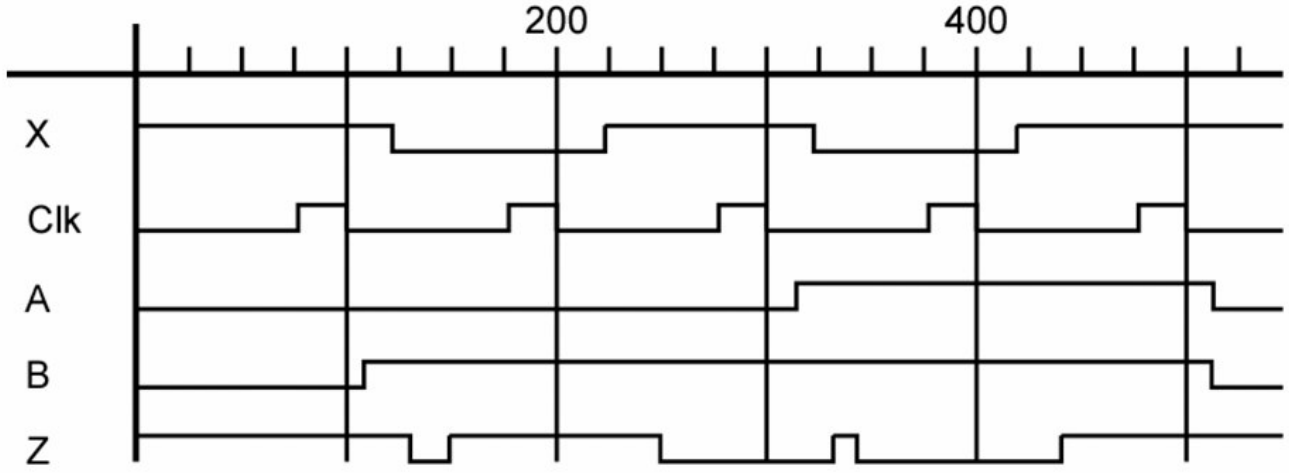


Figure 16-22: **Simulation Screen for Figure 13-7**



(a) Simulator output with a unit delay model



(b) Simulator output with a nominal delay of 10 ns

Figure 16-23

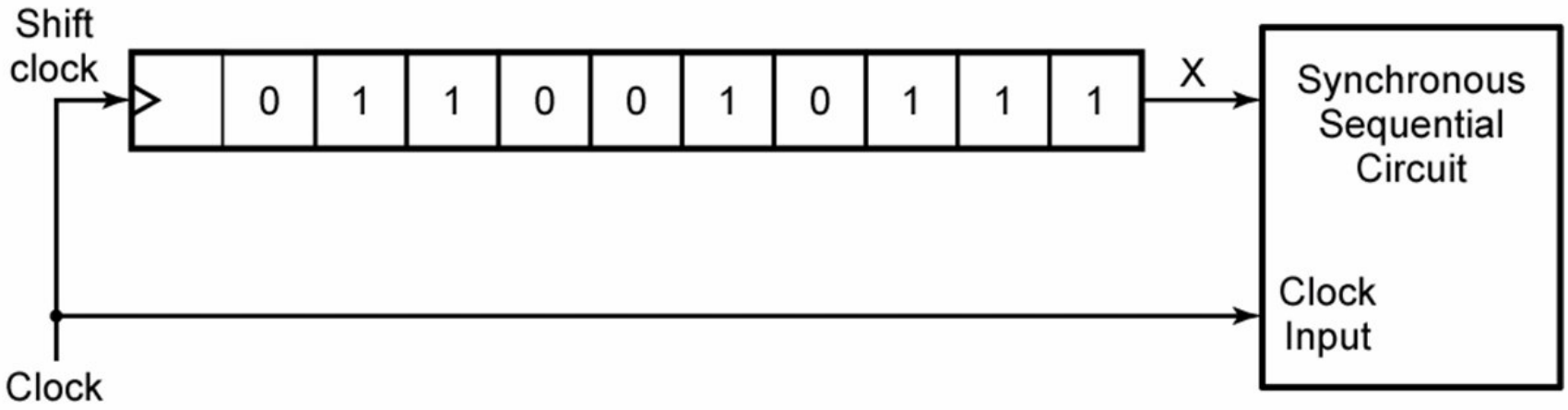
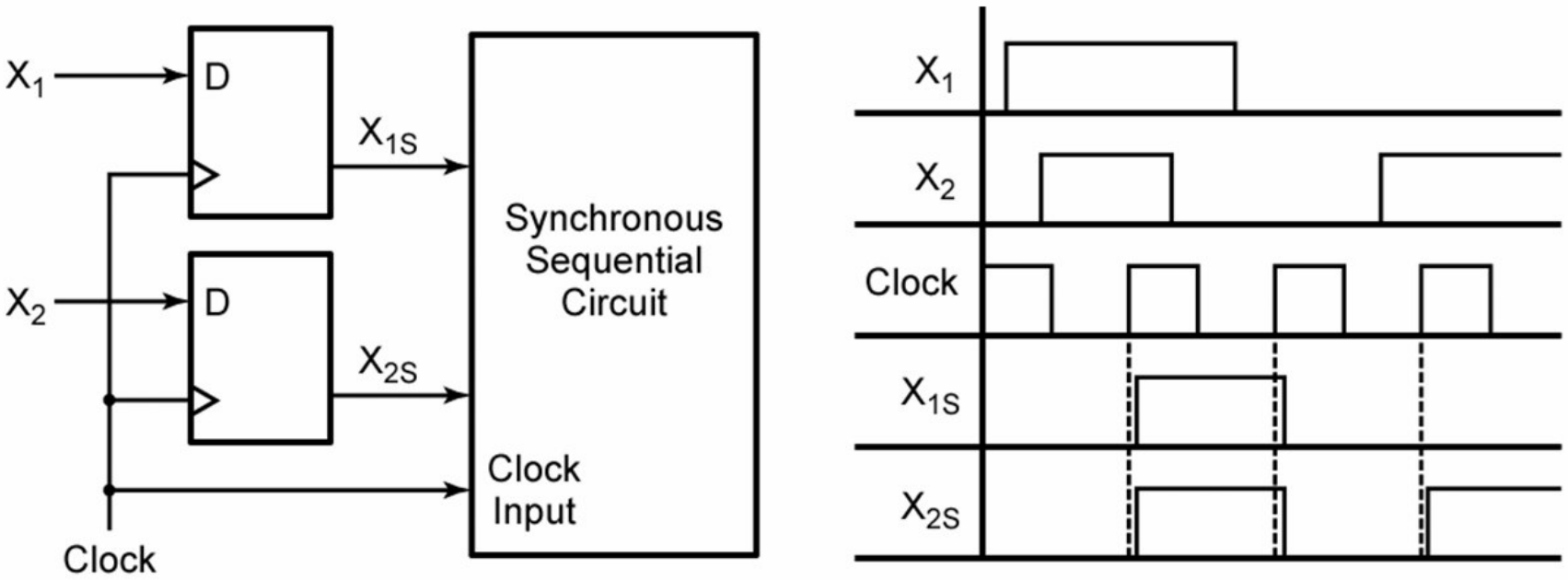


Figure 16-24: **Using a Shift Register to Generate Synchronized Inputs**



(a) Synchronizer circuit

(b) Synchronizer inputs and outputs

Figure 16-25

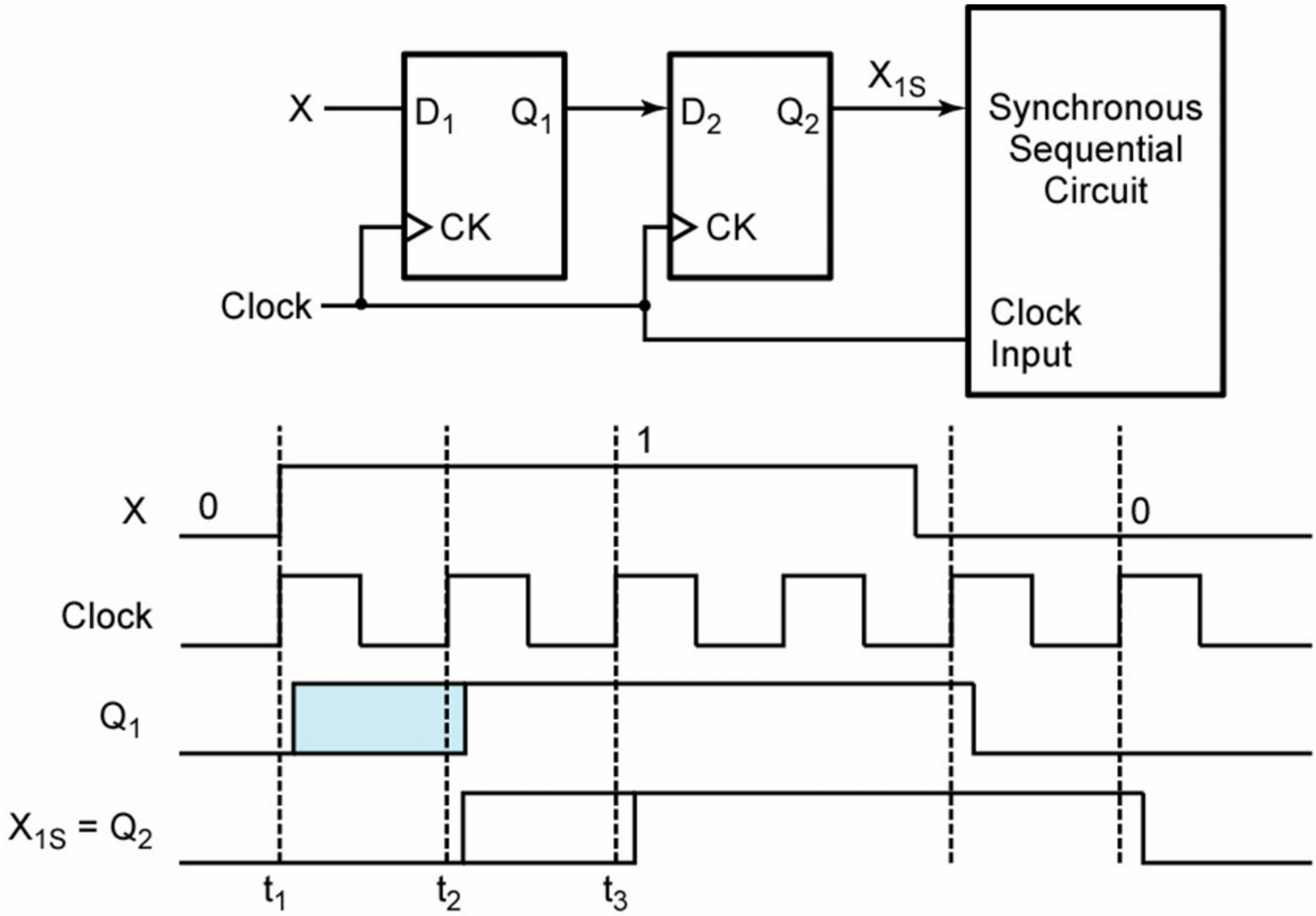


Figure 16-26: **Synchronizer with Two D Flip-Flops**

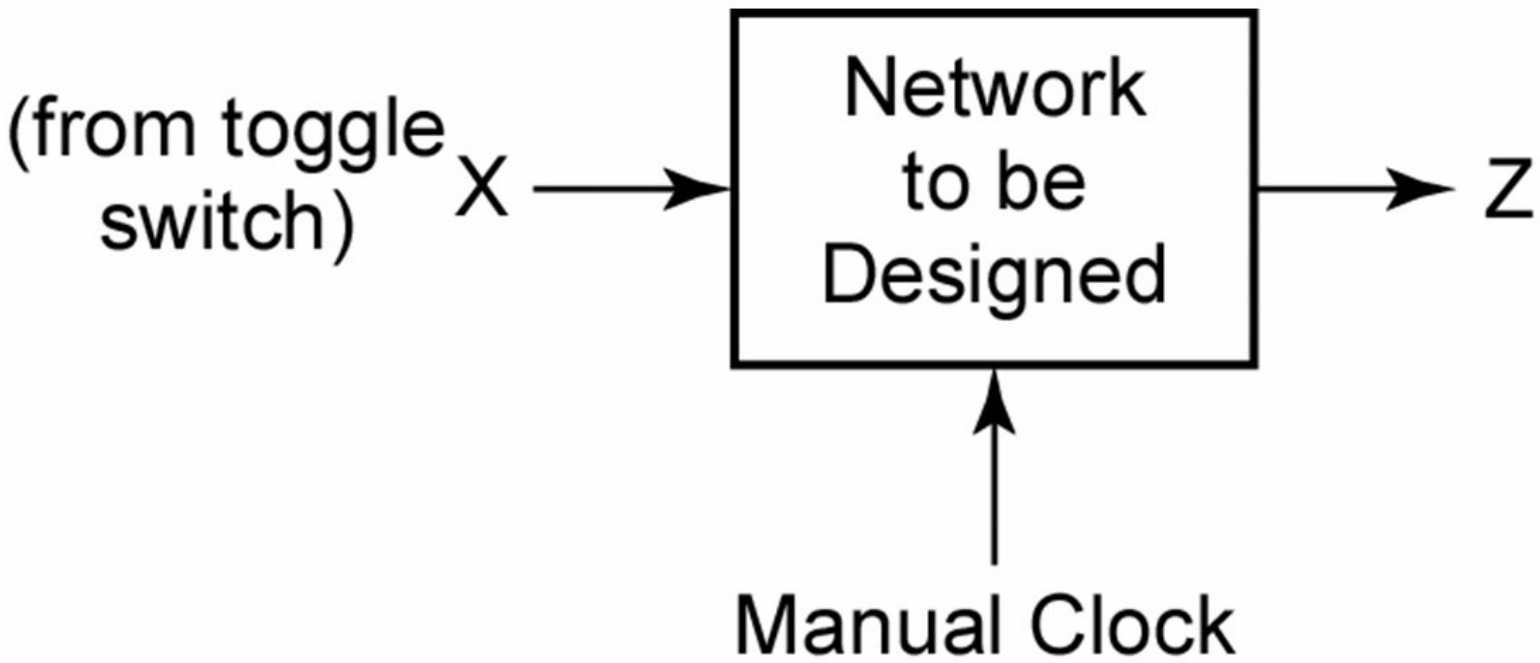


Figure 16-27