FIGURES FOR

CHAPTER 15

REDUCTION OF STATE TABLES
STATE ASSIGNMENT

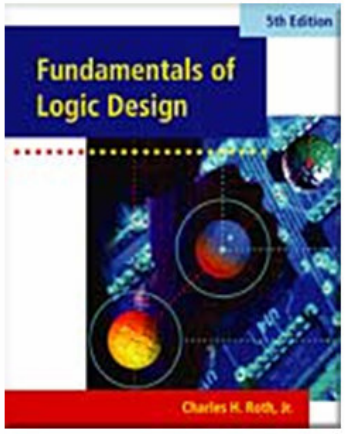

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Table 15-1: State Table for Sequence Detector

Input Sequence	Present State	Next State $X = 0$	Next State $X = 1$	Present Output $X = 0$	Present Output $X = 1$
reset	*A*	*B*	*C*	0	0
0	*B*	*D*	*E*	0	0
1	*C*	*F*	*G*	0	0
00	*D*	*H*	*I*	0	0
01	*E*	*J*	*K*	0	0
10	*F*	*L*	*M*	0	0
11	*G*	*N*	*P*	0	0
000	*H*	*A*	*A*	0	0
001	*I*	*A*	*A*	0	0
010	*J*	*A*	*A*	0	1
011	*K*	*A*	*A*	0	0
100	*L*	*A*	*A*	0	1
101	*M*	*A*	*A*	0	0
110	*N*	*A*	*A*	0	0
111	*P*	*A*	*A*	0	0

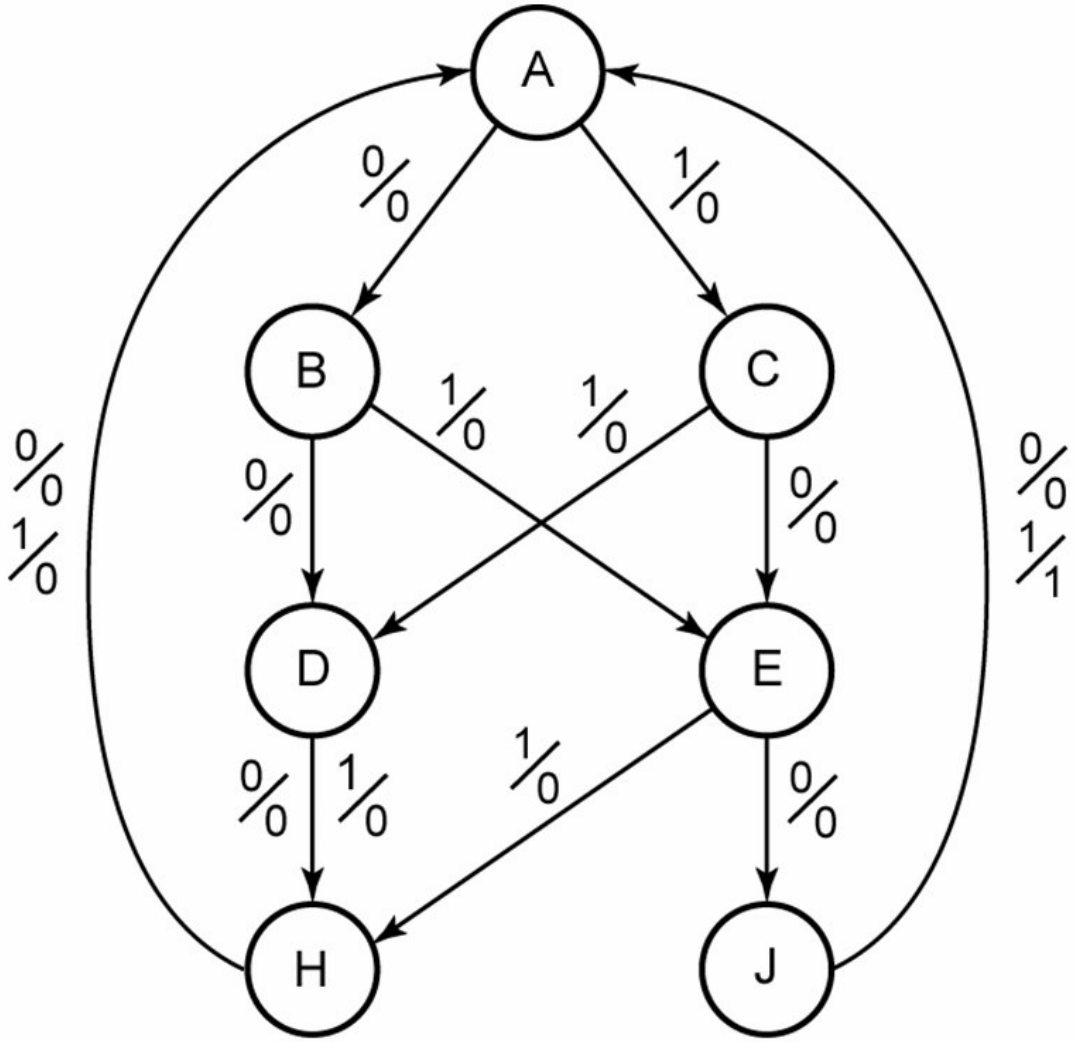
Table 15-2. State Table for Sequence Detector

Present State	Next State $X = 0$	Next State $X = 1$	Present Output $X = 0$	Present Output $X = 1$
A	B	C	0	0
B	D	E	0	0
C	F E	G D	0	0
D	H	I H	0	0
E	J	K H	0	0
~~F~~	~~L J~~	~~M H~~	~~0~~	~~0~~
~~G~~	~~N H~~	~~P H~~	~~0~~	~~0~~
H	A	A	0	0
~~I~~	~~A~~	~~A~~	~~0~~	~~0~~
J	A	A	0	1
~~K~~	~~A~~	~~A~~	~~0~~	~~0~~
~~L~~	~~A~~	~~A~~	~~0~~	~~1~~
~~M~~	~~A~~	~~A~~	~~0~~	~~0~~
~~N~~	~~A~~	~~A~~	~~0~~	~~0~~
~~P~~	~~A~~	~~A~~	~~0~~	~~0~~

Present State	Next State		Output	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
A	B	C	0	0
B	D	E	0	0
C	E	D	0	0
D	H	H	0	0
E	J	H	0	0
H	A	A	0	0
J	A	A	0	1

(a)

Figure 15-1a: **Reduced State Table for Sequence Detector**



(b)

Figure 15-1b: **Reduced State Graph for Sequence Detector**

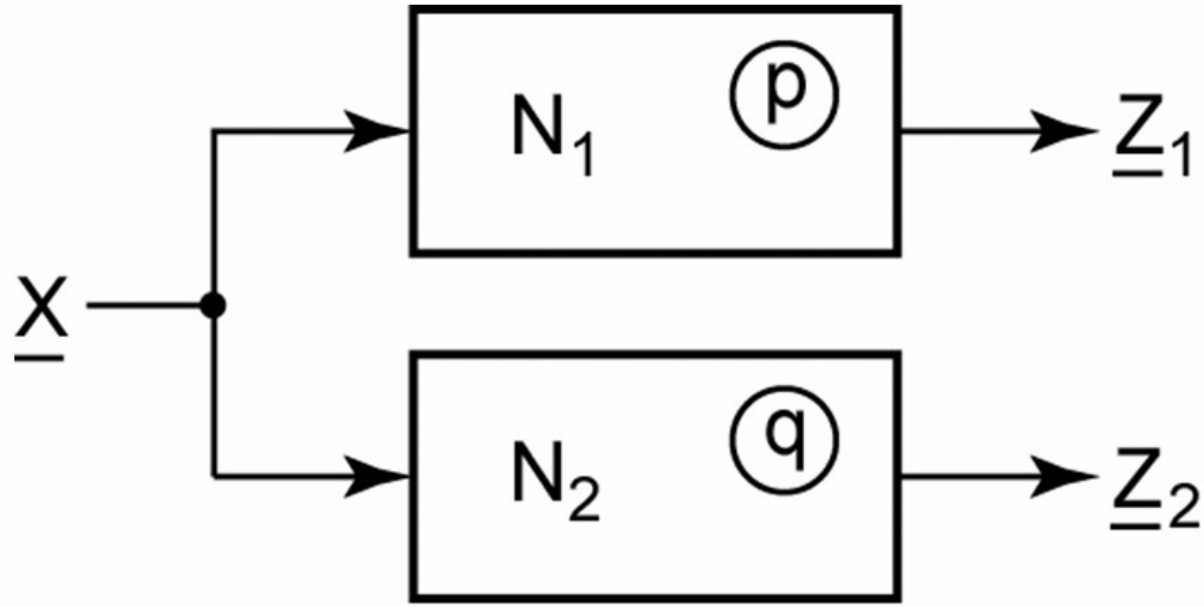


Figure 15-2

Table 15-3.

Present State	Next State $X = 0$	Next State 1	Present Output
a	d	c	0
b	f	h	0
c	e	d	1
d	a	e	0
e	c	a	1
f	f	b	1
g	b	h	0
h	c	g	1

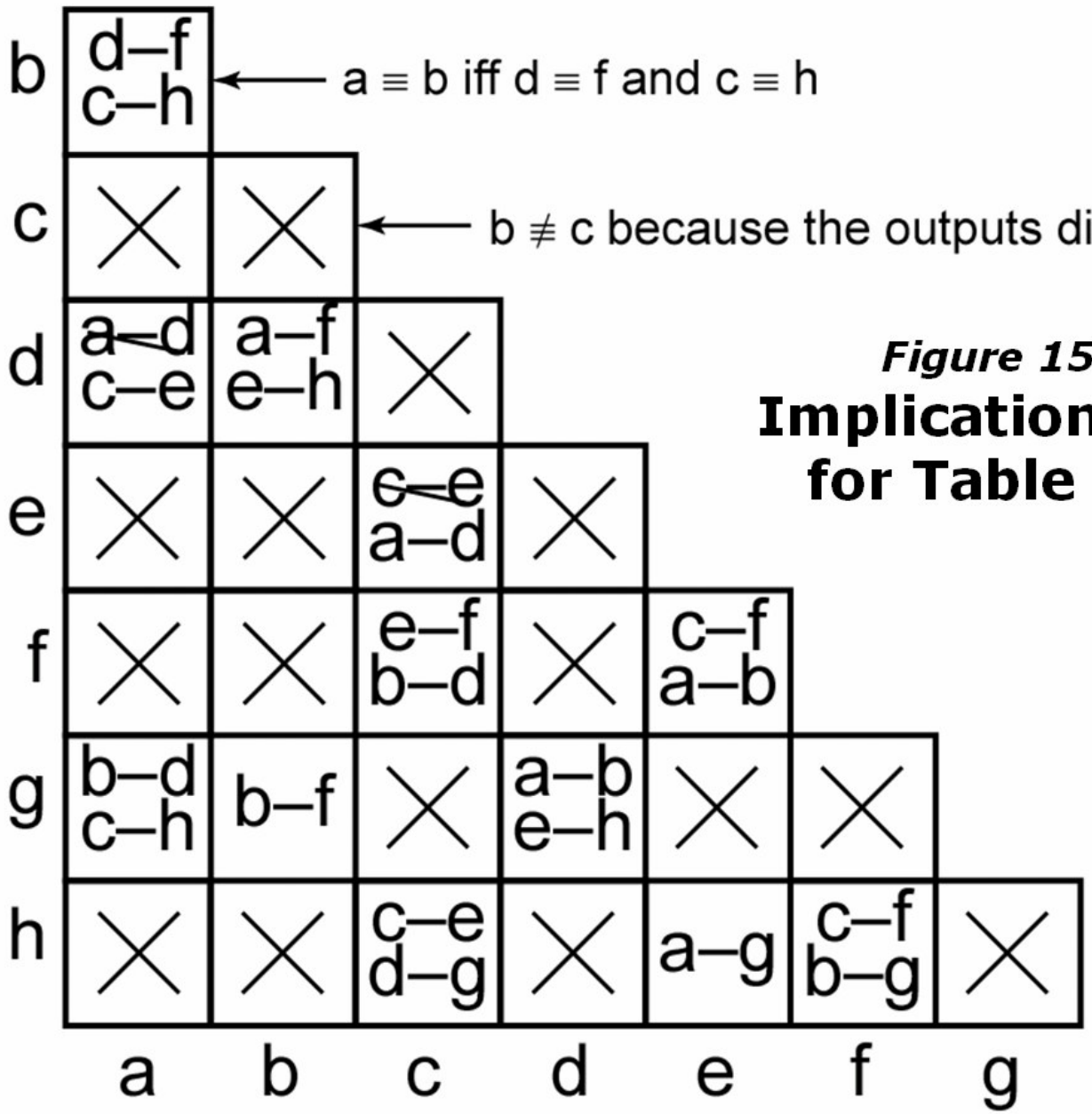


Figure 15-3:

Implication Chart for Table 15-3

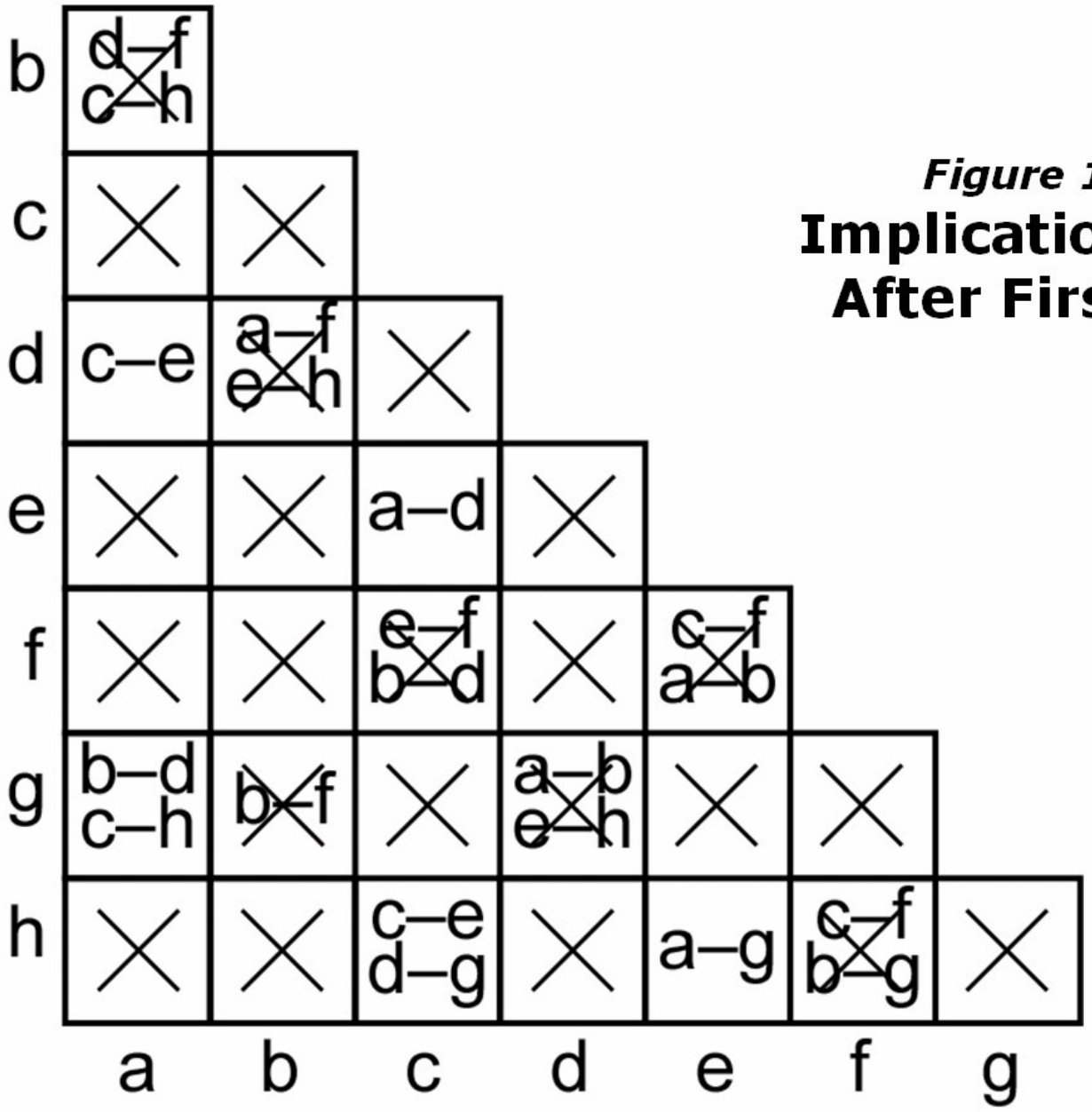


Figure 15-4:

Implication Chart After First Pass

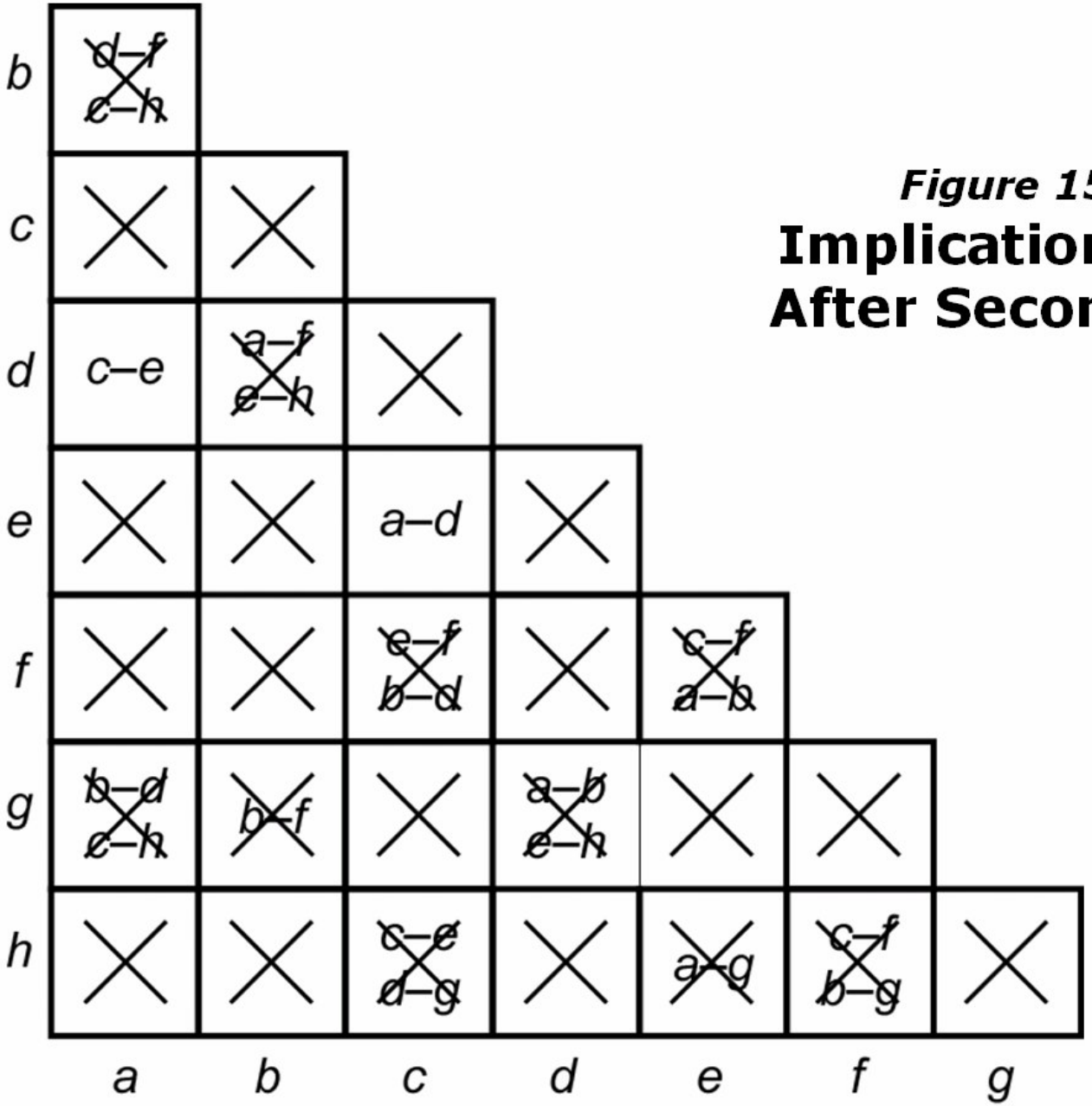


Figure 15-5:

Implication Chart After Second Pass

Table 15-4.

Present State	Next State $X = 0$	Next State 1	Output
a	a	c	0
b	f	h	0
c	c	a	1
f	f	b	1
g	b	h	0
h	c	g	1

	N_1			
	$X = 0$	1	$X = 0$	1
A	B	A	0	0
B	C	D	0	1
C	A	C	0	1
D	C	B	0	0

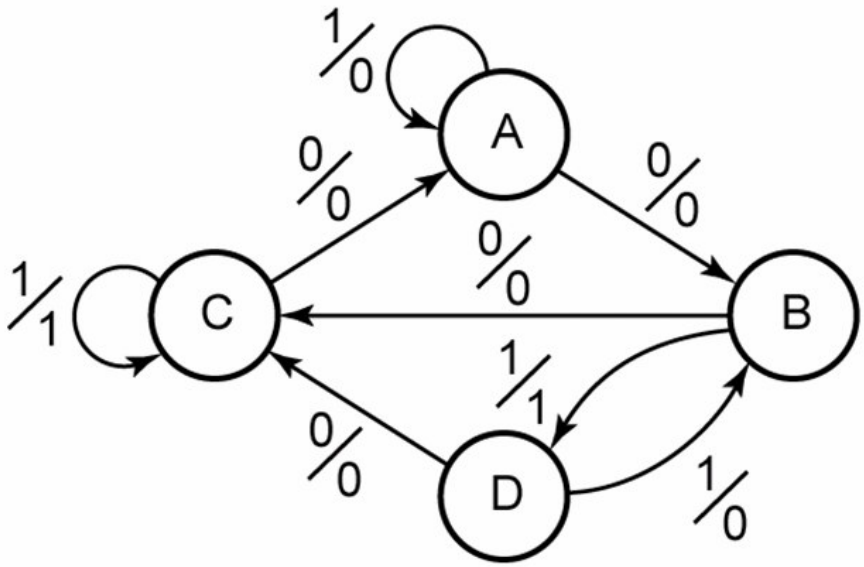


Figure 15-6a: **Graphs for Equivalent Circuits**

	N_2			
	$X = 0$	1	$X = 0$	1
S_0	S_3	S_1	0	1
S_1	S_3	S_0	0	0
S_2	S_0	S_2	0	0
S_3	S_2	S_3	0	1

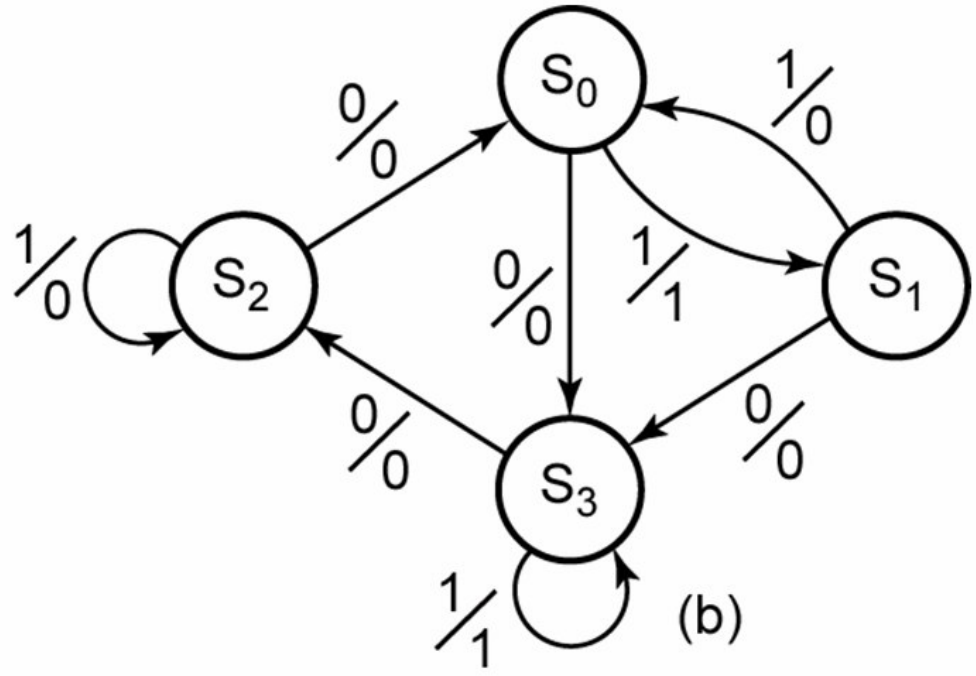


Figure 15-6b: **Graphs for Equivalent Circuits**

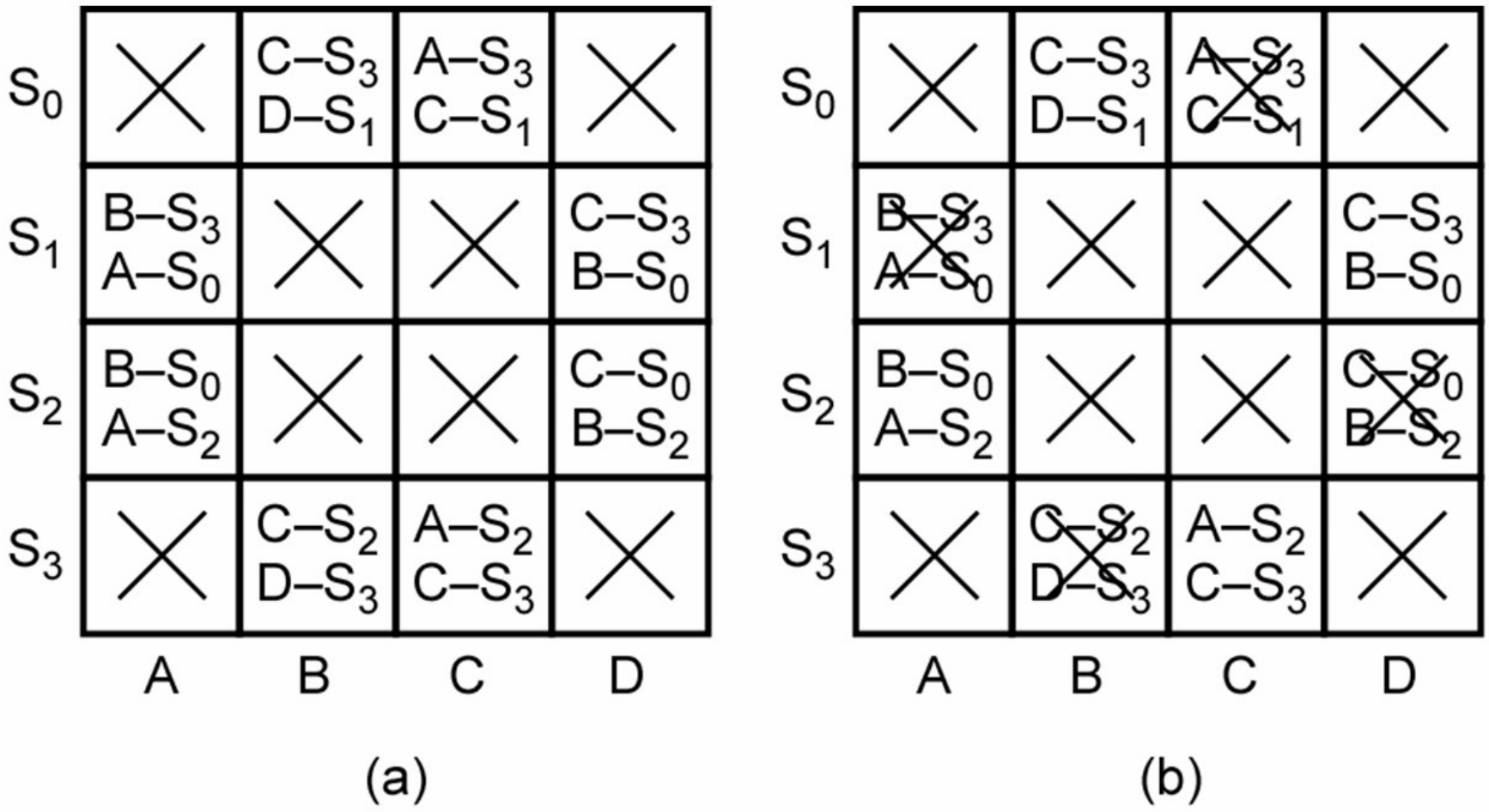


Figure 15-7: **Implication Tables for Determining Circuit Equivalence**

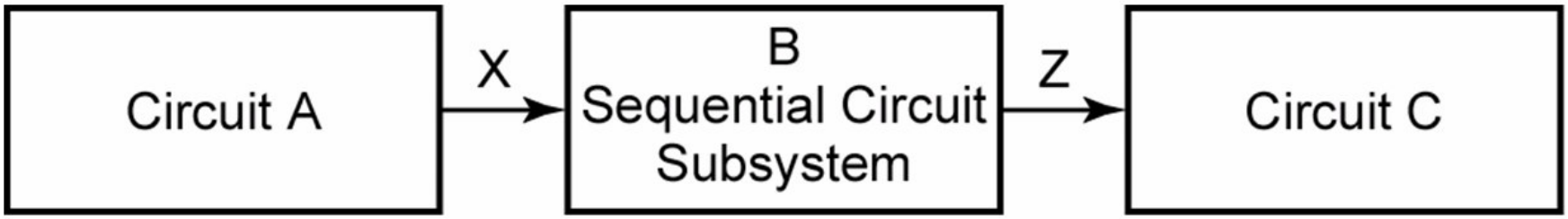


Figure 15-8

Table 15-5. Incompletely Specified State Table

	$X=0$	1	0	1
S_0	–	S_1	–	–
S_1	S_2	S_3	–	–
S_2	S_0	–	0	–
S_3	S_0	–	1	–

(a)

	$X=0$	1	0	1
S_0	(S_0)	S_1	(0)	–
S_1	~~S_2~~ S_0	S_3	(1)	–
S_2	S_0	(S_1)	0	–
S_3	S_0	(S_3)	1	–

(b)

$S_0 \equiv S_2, S_1 \equiv S_3$

(c)

	$X=0$	1	0	1
S_0	S_0	S_1	0	–
S_1	S_0	S_1	1	–

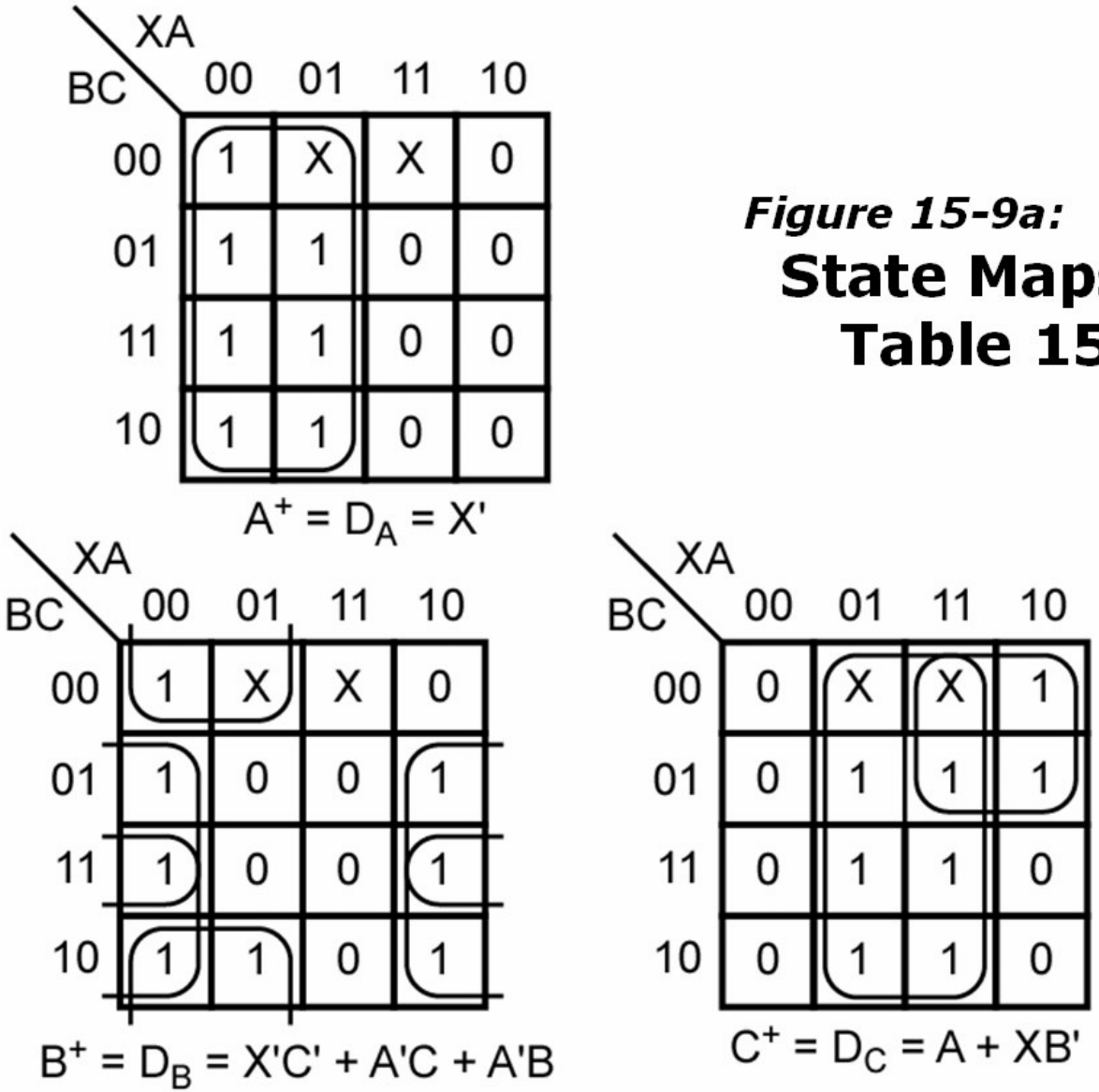
Table 15-6.

(a) state table

	X = 0	1	0	1
S_0	S_1	S_2	0	0
S_1	S_3	S_2	0	0
S_2	S_1	S_4	0	0
S_3	S_5	S_2	0	0
S_4	S_1	S_6	0	0
S_5	S_5	S_2	1	0
S_6	S_1	S_6	0	1

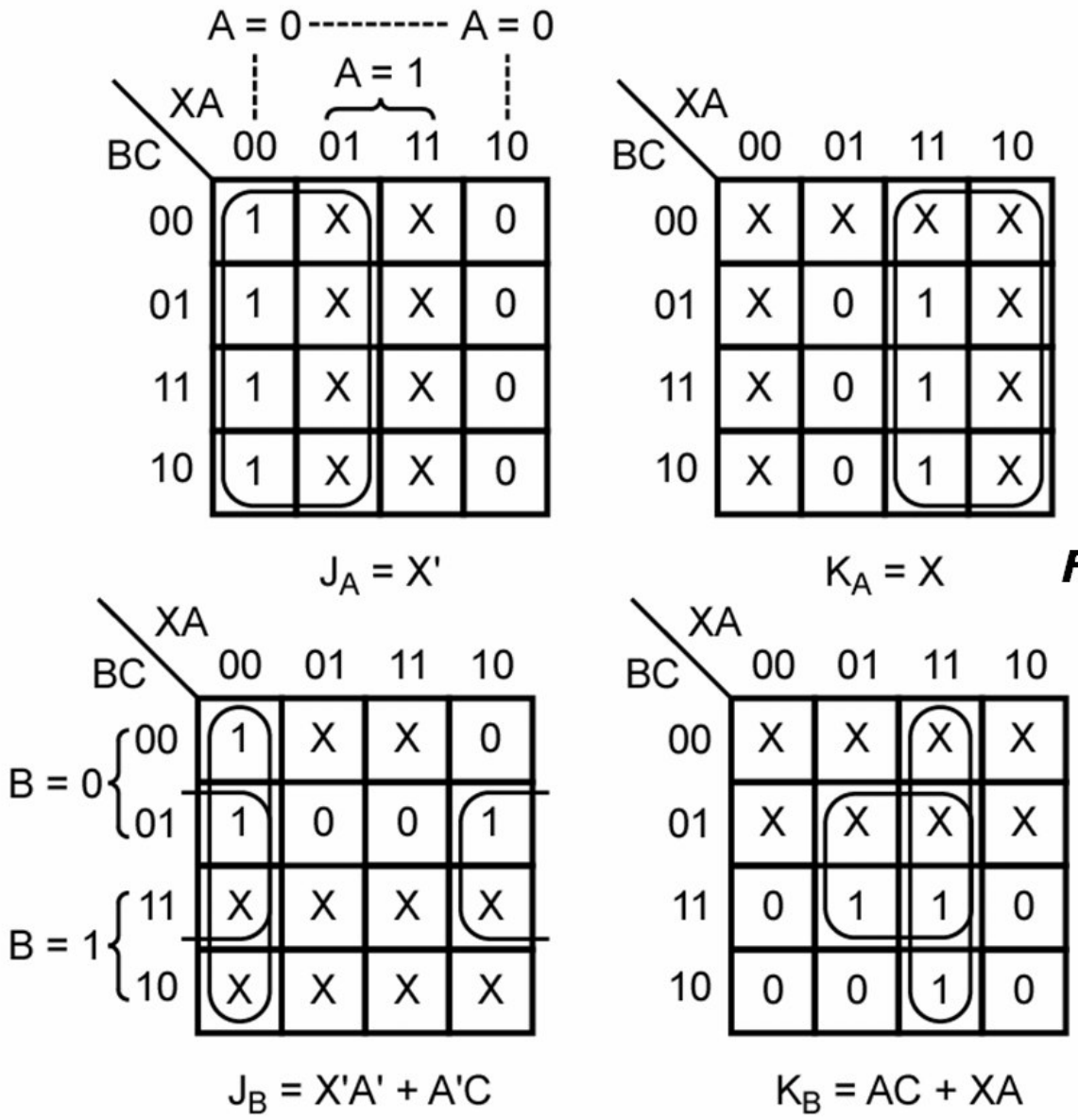
(b) transition table

	$A^+B^+C^+$		Z	
ABC	$X = 0$	1	0	1
000	110	001	0	0
110	111	001	0	0
001	110	011	0	0
111	101	001	0	0
011	110	010	0	0
101	101	001	1	0
010	110	010	0	1



(a) Derivation of D flip-flop input equations

Figure 15-9a: **Next-State Maps for Table 15-6**



(b) Derivation of J-K flip-flop input equations

Figure 15-9b: **Next-State Maps for Table 15-6**

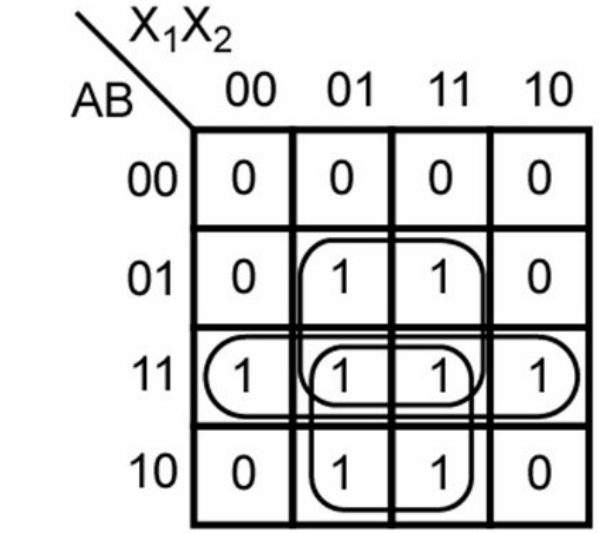
Table 15-7.

(a) state table

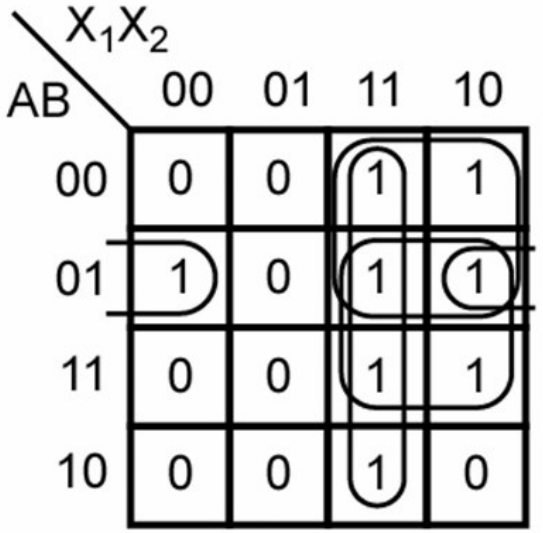
P.S.	Next State $X_1X_2 =$ 00	01	11	10	Outputs (Z_1Z_2) $X_1X_2 =$ 00	01	11	10
S_0	S_0	S_0	S_1	S_1	00	00	01	01
S_1	S_1	S_3	S_2	S_1	00	10	10	00
S_2	S_3	S_3	S_2	S_2	11	11	00	00
S_3	S_0	S_3	S_2	S_0	00	00	00	00

(b) transition table

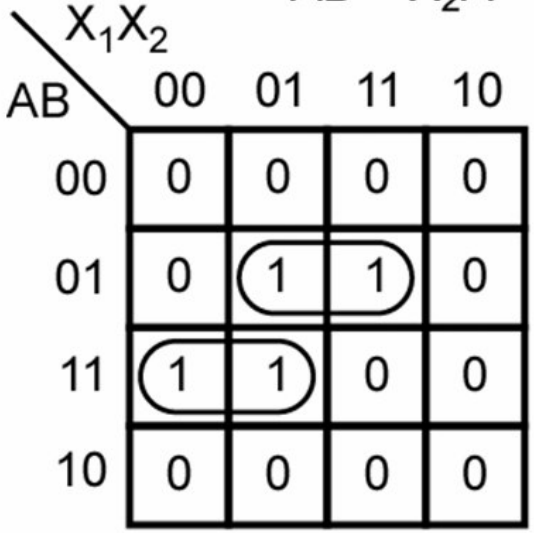
AB	A^+B^+ $X_1X_2 =$ 00	01	11	10	Outputs (Z_1Z_2) $X_1X_2 =$ 00	01	11	10
00	00	00	01	01	00	00	01	01
01	01	10	11	01	00	10	10	00
11	10	10	11	11	11	11	00	00
10	00	10	11	00	00	00	00	00



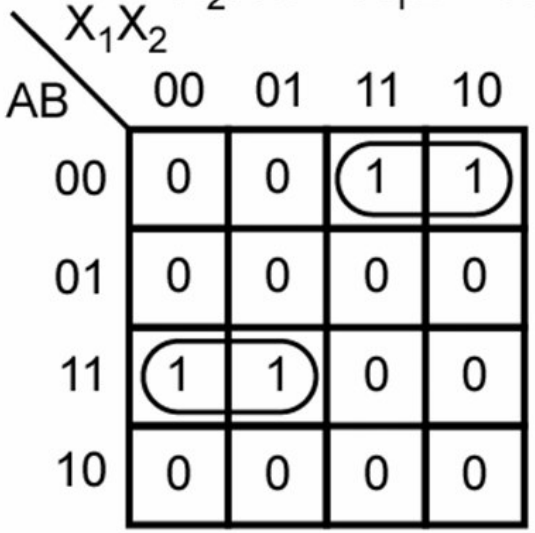
$D_A = A^+ = X_2B + AB + X_2A$



$D_B = B^+ = X_1A' + X_2A'B + X_1B + X_1X_2$



$Z_1 = X_2A'B + X_1'AB$



$Z_2 = X_1A'B' + X_1'AB$

Figure 15-10:

Next-State Maps for Table 15-7

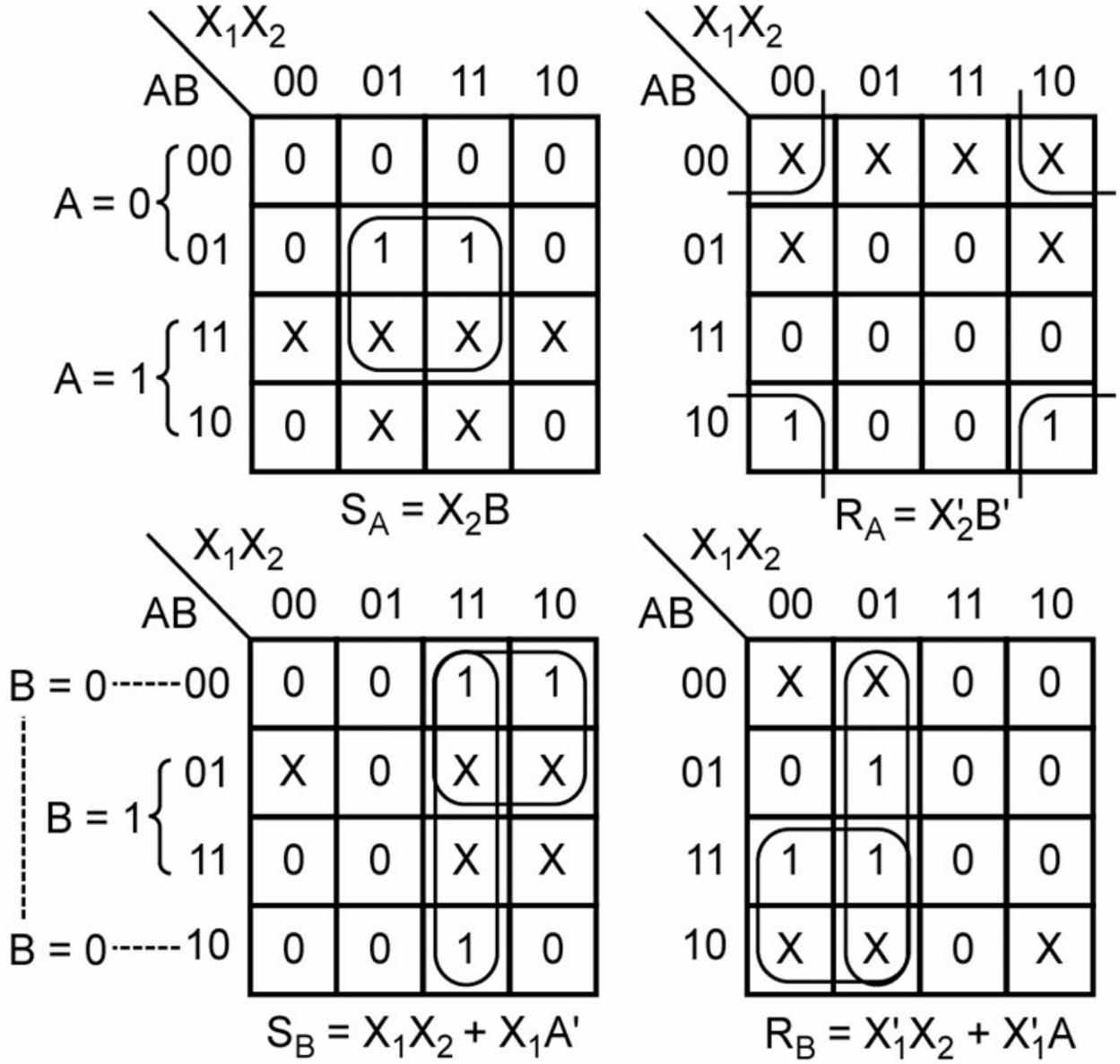
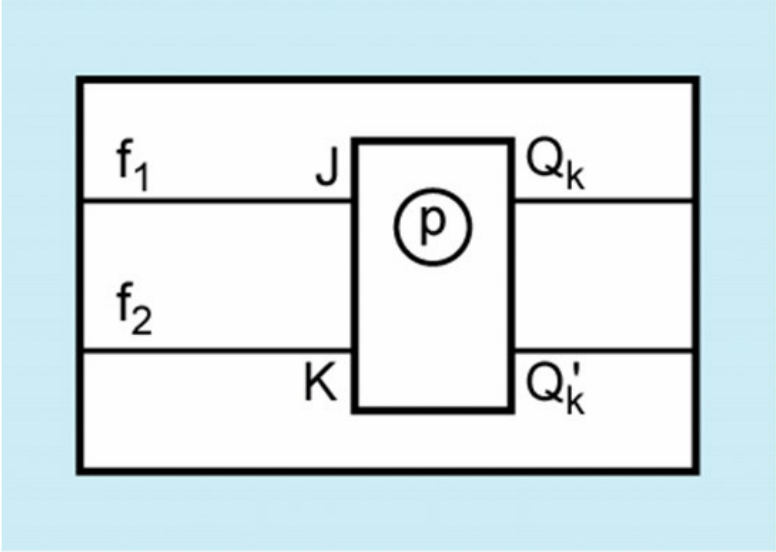


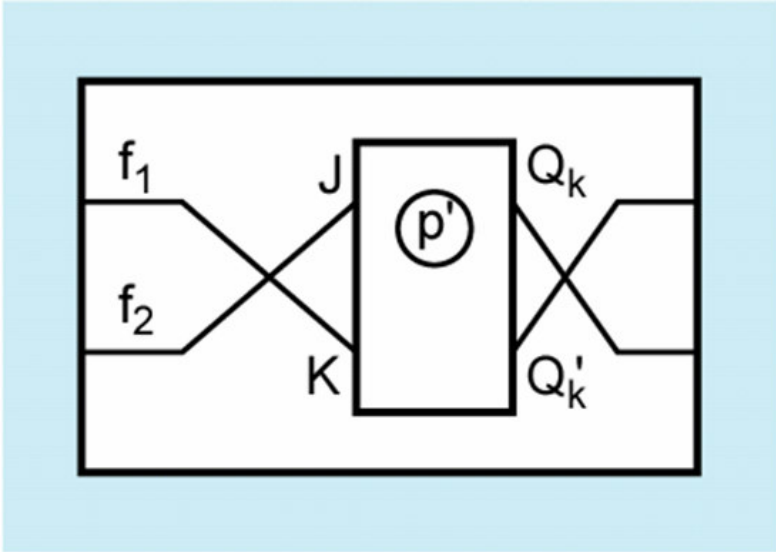
Figure 15-11: **Derivation of S-R Equations for Table 15-7**

Table 15-8. State Assignments for 3-Row Tables

	1	2	3	4	5	6	7	···	19	20	21	22	23	24
S_0	00	00	00	00	00	00	01	···	11	11	11	11	11	11
S_1	01	01	10	10	11	11	00		00	00	01	01	10	10
S_2	10	11	01	11	01	10	10		01	10	00	10	00	01

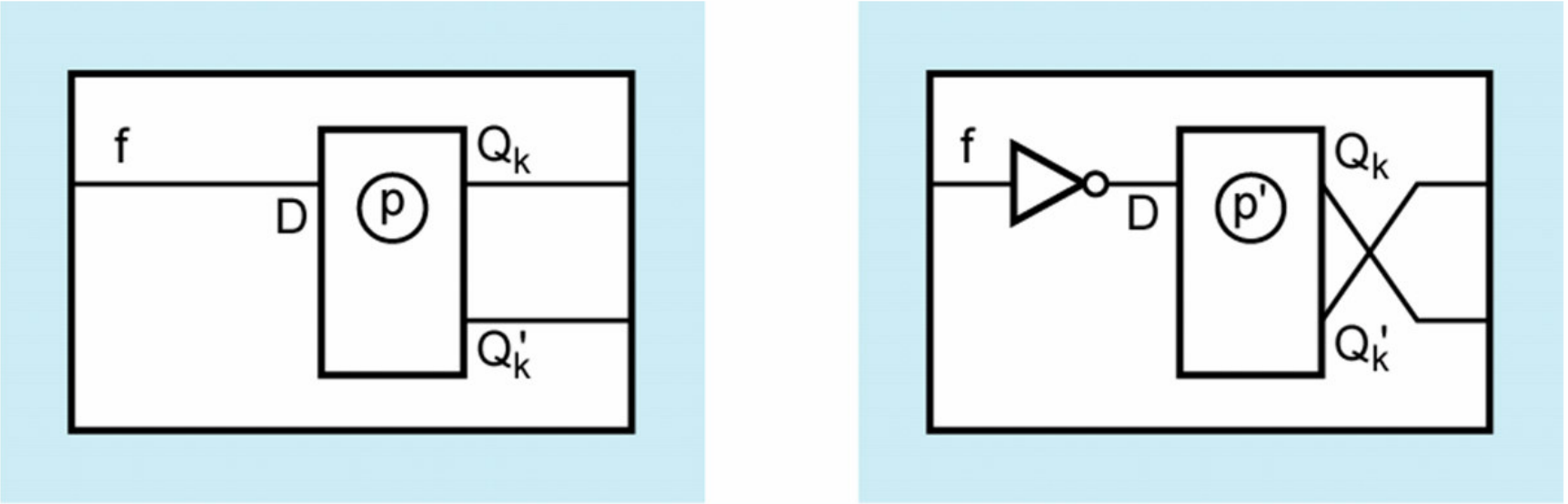


(a) Circuit A



(b) Circuit B
(identical to A except
leads to flip-flop Q_k are crossed)

Figure 15-12: **Equivalent Circuits Obtained by Complementing Q_k**



(a) Circuit A

(b) Circuit B
(identical to A except for
connections to flip-flop Q_k)

Figure 15-13: **Equivalent Circuits Obtained by Complementing Q_k**

Table 15-9.

Assignments A_3	B_3	C_3	Present State	Next State $X = 0$	1	Output 0	1
00	00	11	S_1	S_1	S_3	0	0
01	10	10	S_2	S_2	S_1	0	1
10	01	01	S_3	S_2	S_3	1	0

Assignment “A“	Assignment “B"	Assignment “C"
$J_1 = XQ'_2$	$J_2 = XQ_1'$	$K_1 = XQ_2$
$K_1 = X'$	$K_2 = X'$	$J_1 = X'$
$J_2 = X'Q_1$	$J_1 = X'Q_2$	$K_2 = X'Q_1'$
$K_2 = X$	$K_1 = X$	$J_2 = X$
$Z = X'Q_1 + XQ_2$	$Z = X'Q_2 + XQ_1$	$Z = X'Q_1' + XQ_2'$

$D_1 = XQ_2'$	$D_2 = XQ_1'$	$D_1 = X' + Q_2'$
$D_2 = X'(Q_1+Q_2)$	$D_1 = X'(Q_2 + Q_1)$	$D_2 = X + Q_1Q_2$

Flip-Flop Input Equations

Table 15-10. Nonequivalent Assignments for 3 and 4 States

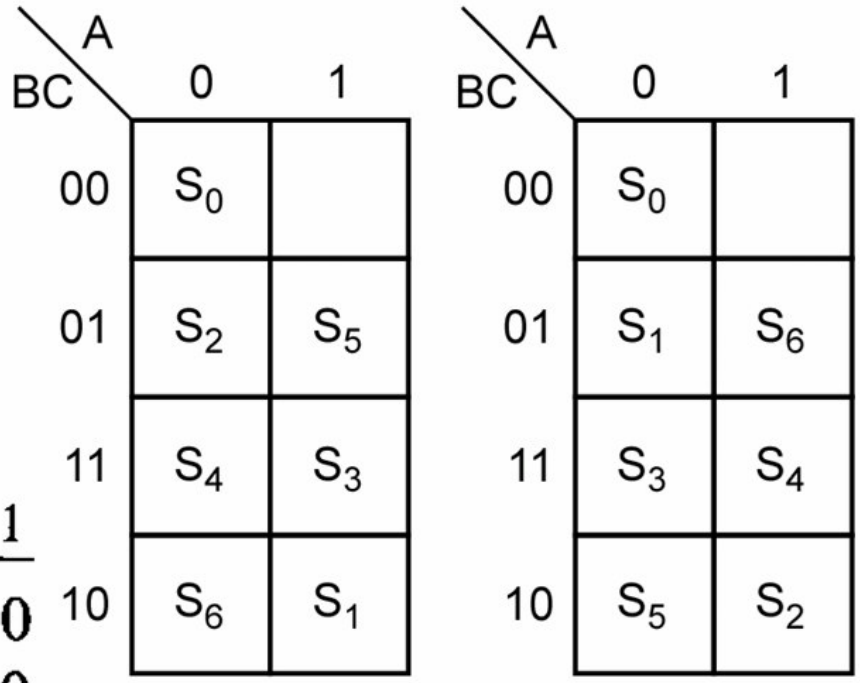
	3-State Assignments			4-State Assignments		
States	1	2	3	1	2	3
a	00	00	00	00	00	00
b	01	01	11	01	01	11
c	10	11	01	10	11	01
d	--	--	--	11	10	10

Table 15-11. Number of Distinct (Nonequivalent) State Assignments

No. of States	Minimum No. of State Variables	No. of Distinct Assignments
2	1	1
3	2	3
4	2	3
5	3	140
6	3	420
7	3	840
8	3	840
9	4	10,810,800
⋮	⋮	⋮
16	4	$\approx 5.5 \times 10^{10}$

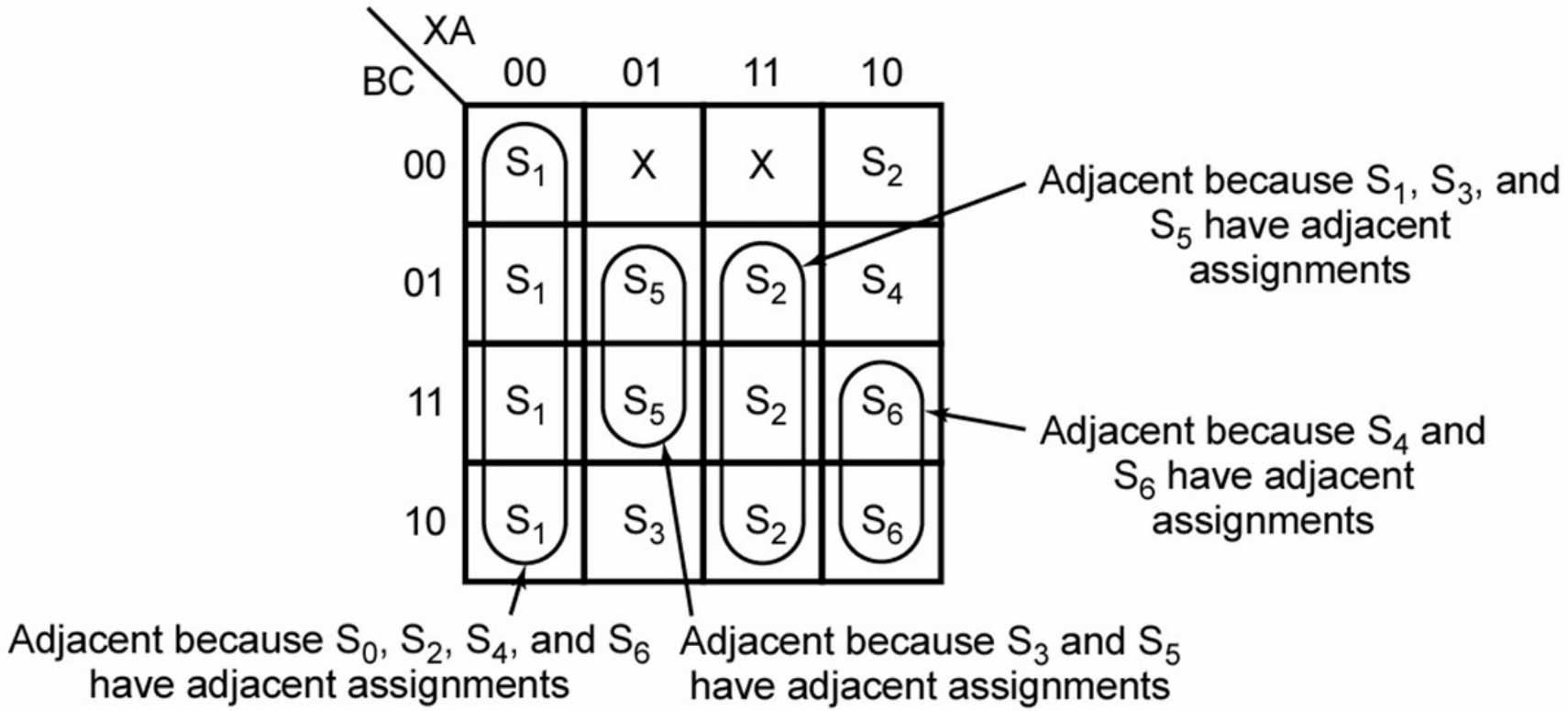
ABC		$X = 0$	1	0	1
000	S_0	S_1	S_2	0	0
110	S_1	S_3	S_2	0	0
001	S_2	S_1	S_4	0	0
111	S_3	S_5	S_2	0	0
011	S_4	S_1	S_6	0	0
101	S_5	S_5	S_2	1	0
010	S_6	S_1	S_6	0	1

(a) state table



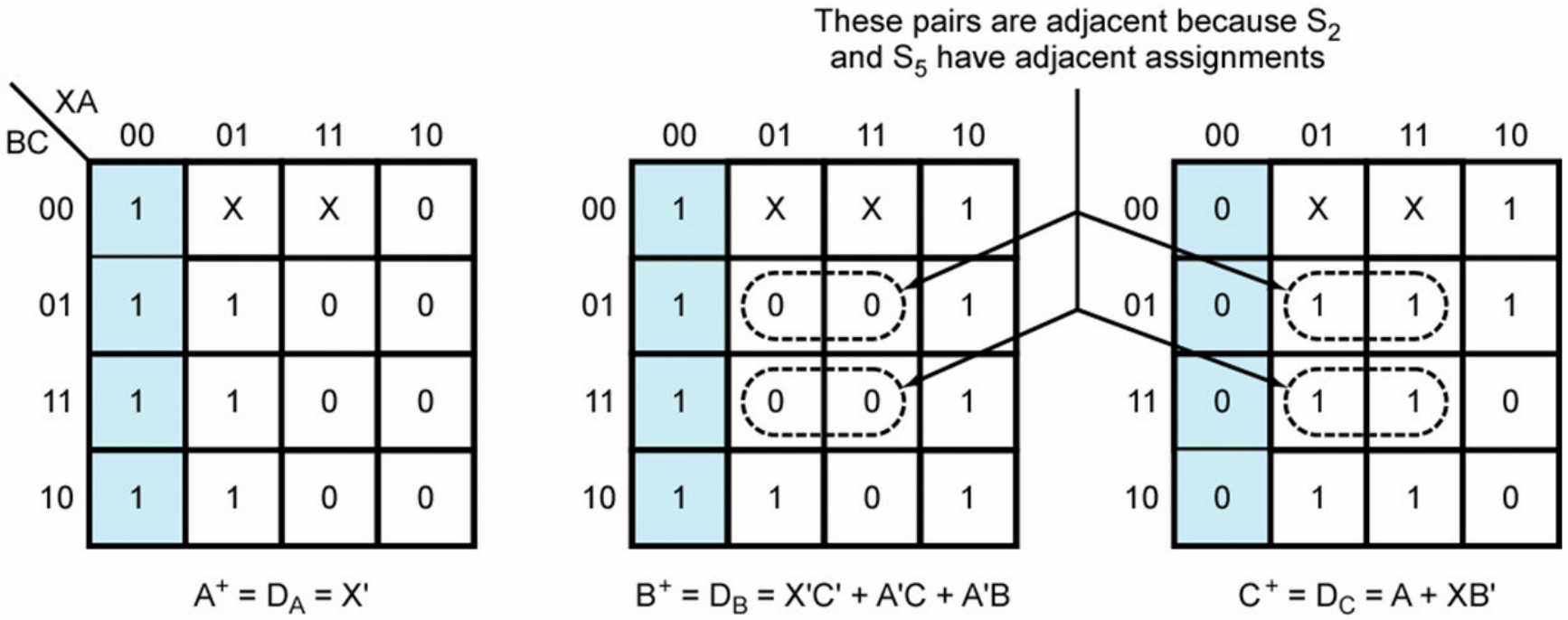
(b) Assignment maps

Figure 15-14b



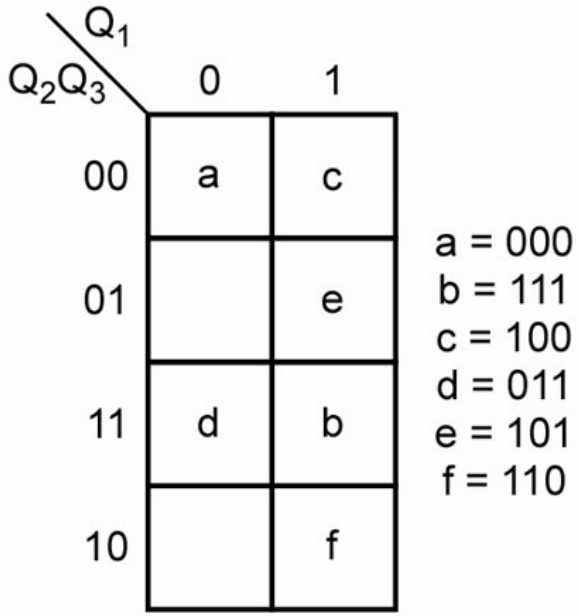
(a) Next-state maps for Figure 15-14

Figure 15-15a: **Next-State Maps for Figure 15-14**

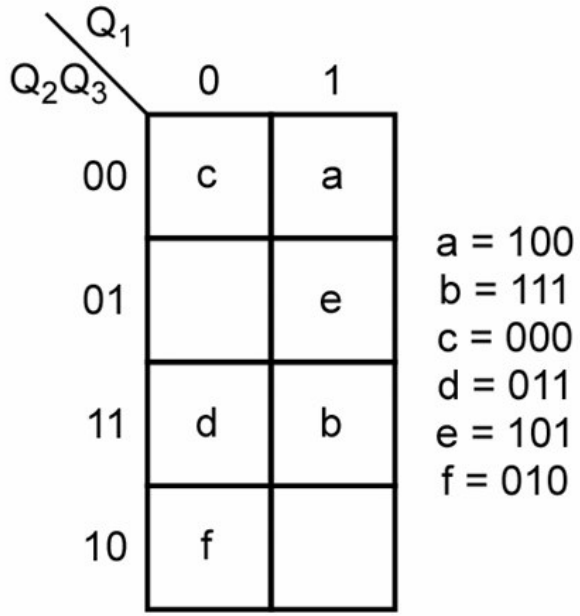


(b) Next-state maps for Figure 15-14 (cont.)

Figure 15-15b: Next-State Maps for Figure 15-14



(b)



(c)

	$X = 0$	1	$X = 0$	1
a	*a*	*c*	0	0
b	*d*	*f*	0	1
c	*c*	*a*	0	0
d	*d*	*b*	0	1
e	*b*	*f*	1	0
f	*c*	*e*	1	0

(a)

Figure 15-16: **State Table and Assignments**

Table 15-12. Transition table for Figure 15-16(a)

	$Q_1^+ Q_2^+ Q_3^+$			
$Q_1 Q_2 Q_3$	$X = 0$	1	$X = 0$	1
1 0 0	100	000	0	0
1 1 1	011	010	0	1
0 0 0	000	100	0	0
0 1 1	011	111	0	1
1 0 1	111	010	1	0
0 1 0	000	101	1	0

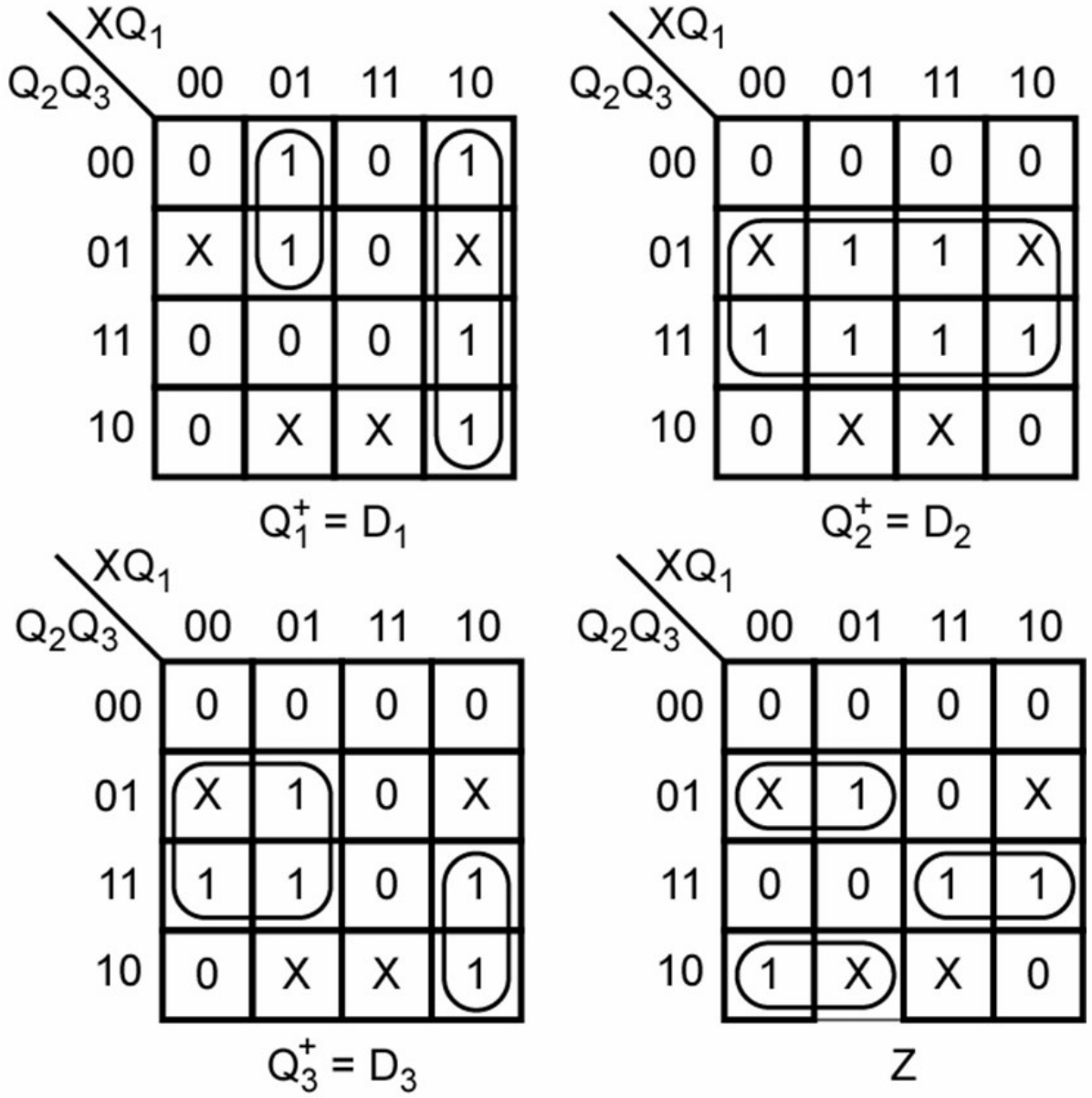


Figure 15-17: **Next-State and Output Maps for Table 15-12**

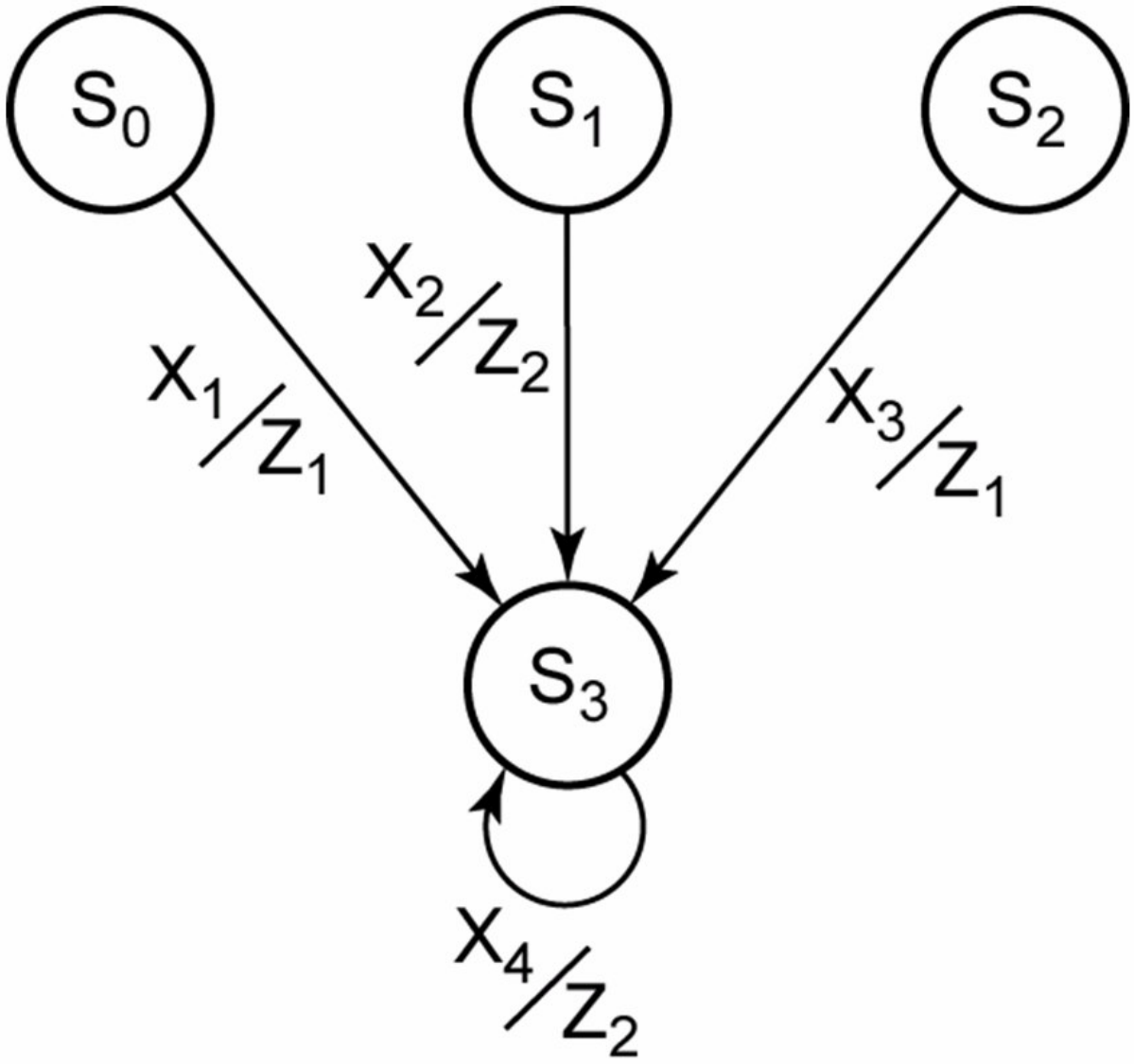


Figure 15-18: **Partial State Graph**