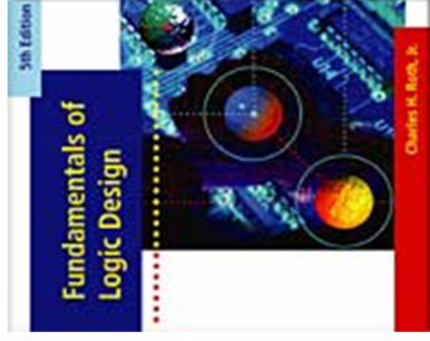


FIGURES FOR CHAPTER 14

DERIVATION OF STATE GRAPHS AND TABLES



This chapter in the book includes:

- Objectives
- Study Guide
- 14.1 Design of a Sequence Detector
- 14.2 More Complex Design Problems
- 14.3 Guidelines for Construction of State Graphs
- 14.4 Serial Data Code Conversion
- 14.5 Alphanumeric State Graph Notation
- Programmed Exercises
- Problems

Click the mouse to move to the next page.
Use the ESC key to exit this chapter.

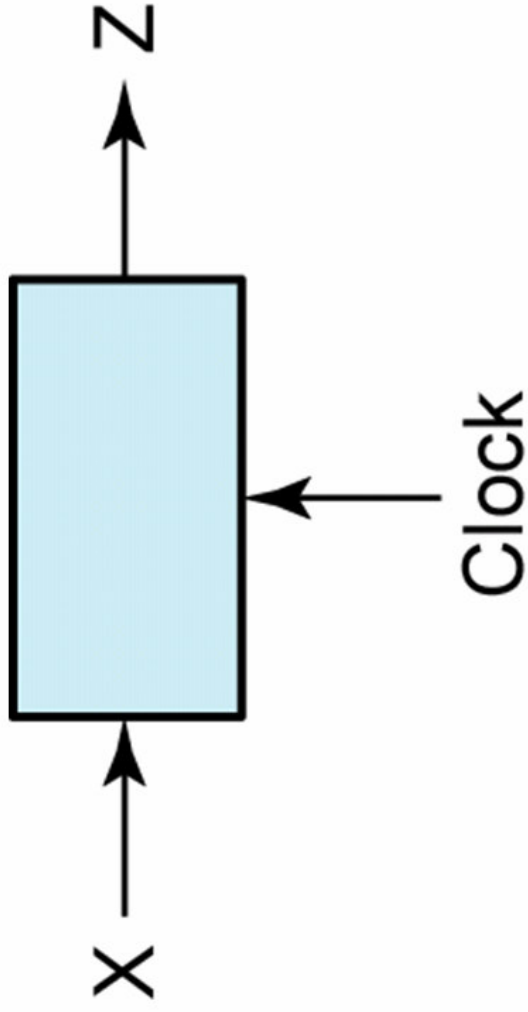


Figure 14-1: Sequence Detector to be Designed

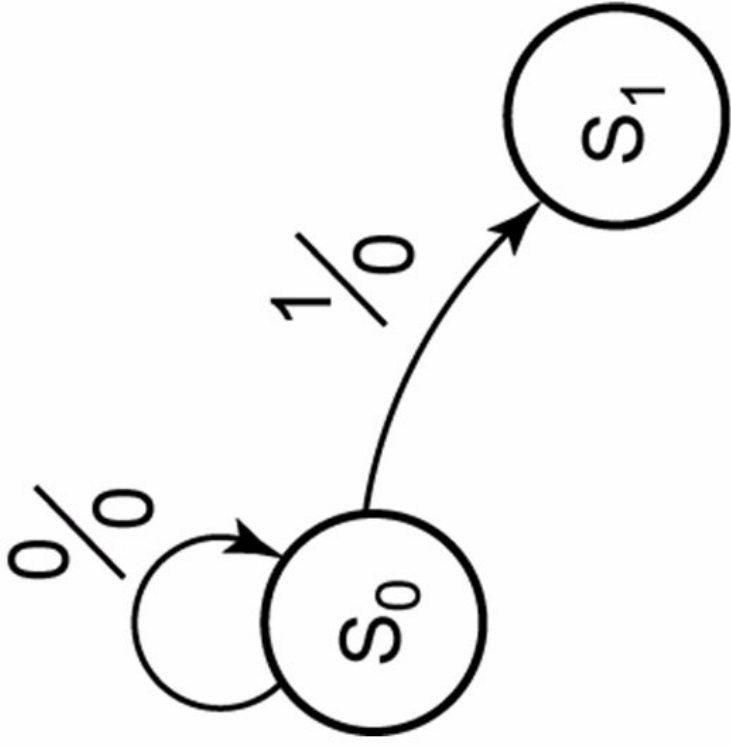


Figure 14-2

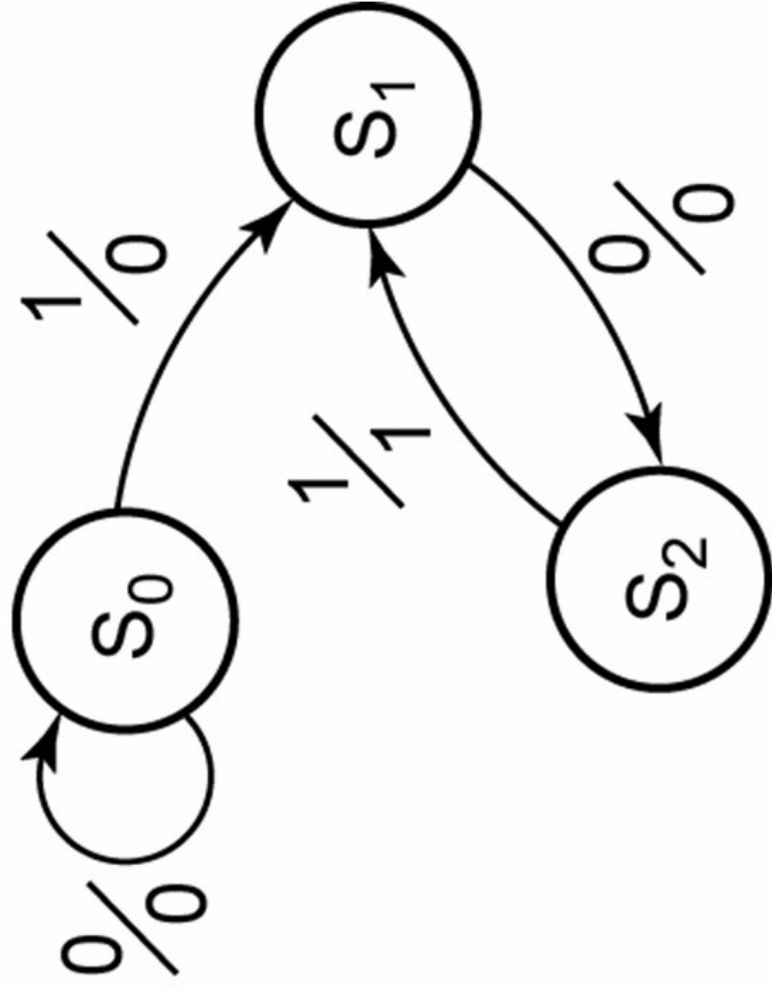


Figure 14-3



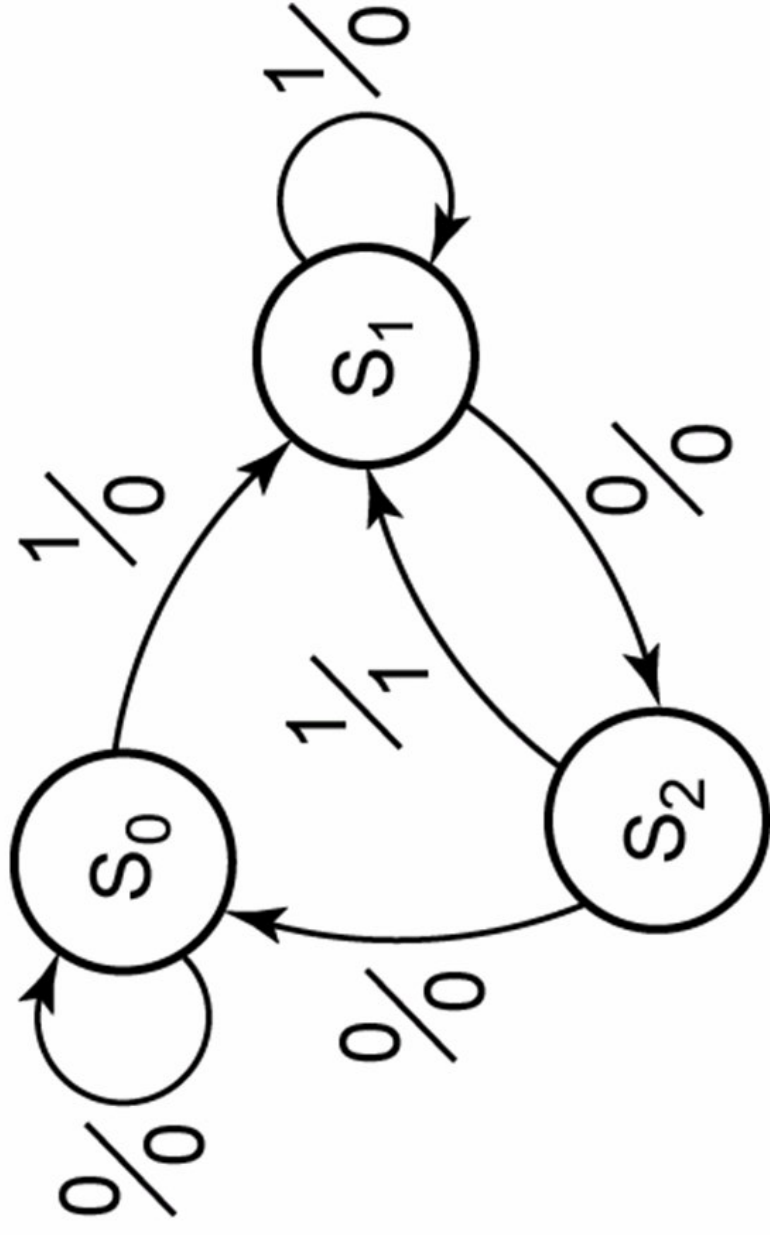


Figure 14-4: Mealy State Graph for Sequence Detector

Table 14-1 and Table 14-2

Present State	Next State		Present Output	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
S_0	S_0	S_1	0	0
S_1	S_2	S_1	0	0
S_2	S_0	S_1	0	1

AB	A^+B^+		Z	
	$X = 0$	$X = 1$	$X = 0$	$X = 1$
00	00	01	0	0
01	10	01	0	0
10	00	01	0	1

X	0	1		
AB	00	01	11	10
	0	1	X	0
	0	0	0	0

$A^+ = X'B$

X	0	1		
AB	00	01	11	10
	0	0	X	0
	1	1	X	1

$B^+ = X$

X	0	1		
AB	00	01	11	10
	0	0	X	0
	0	0	X	1

$Z = XA$

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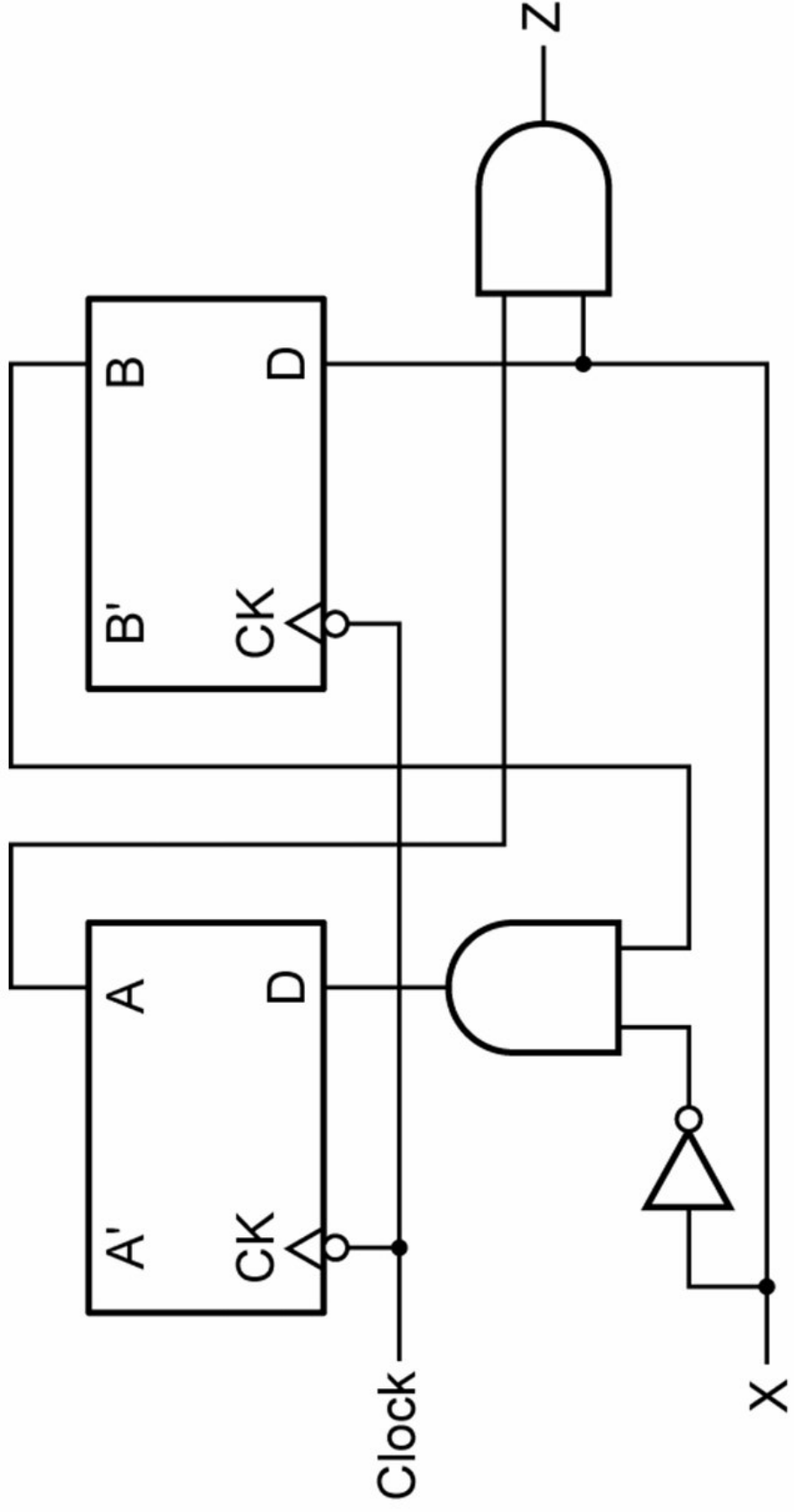
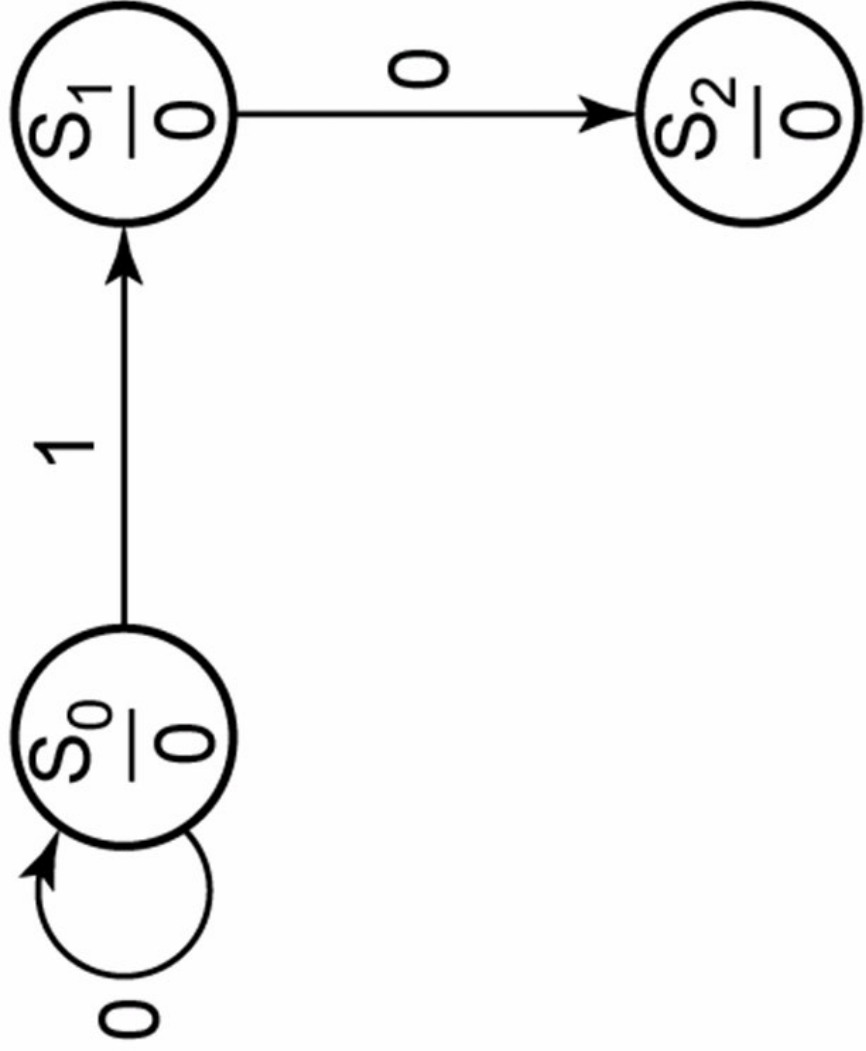
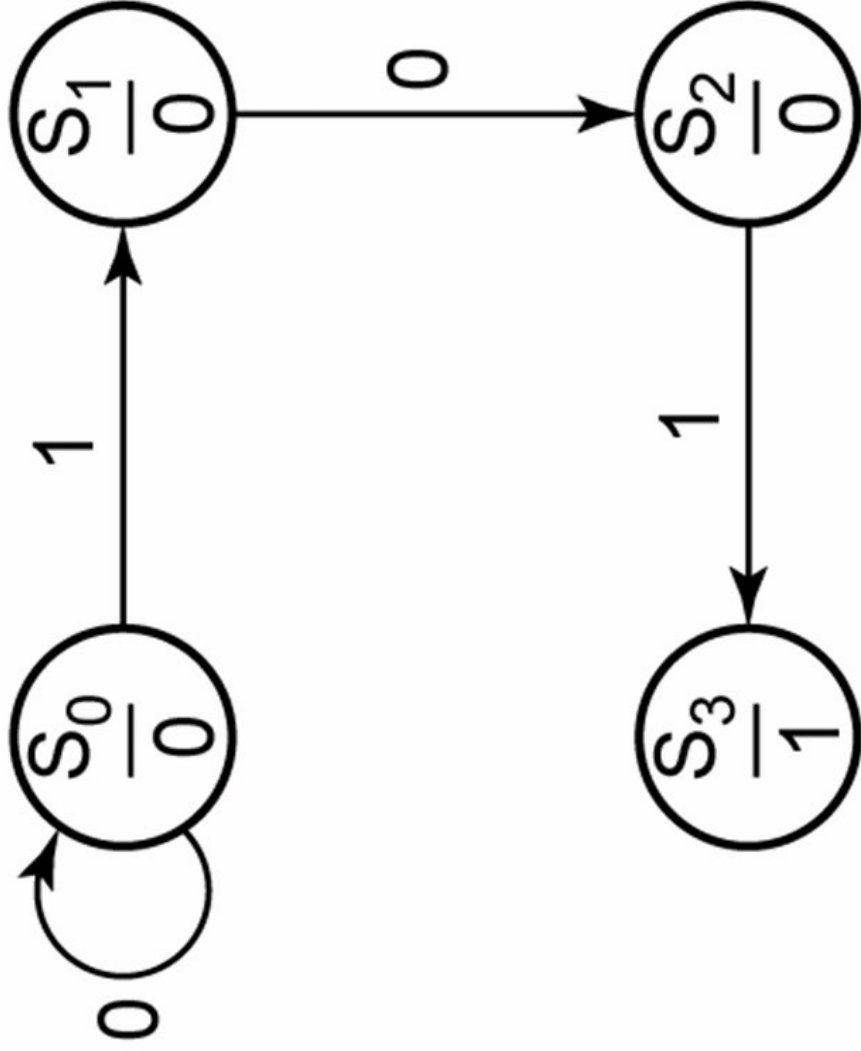


Figure 14-5



Section 14.1, p. 396





Section 14.1, p. 397



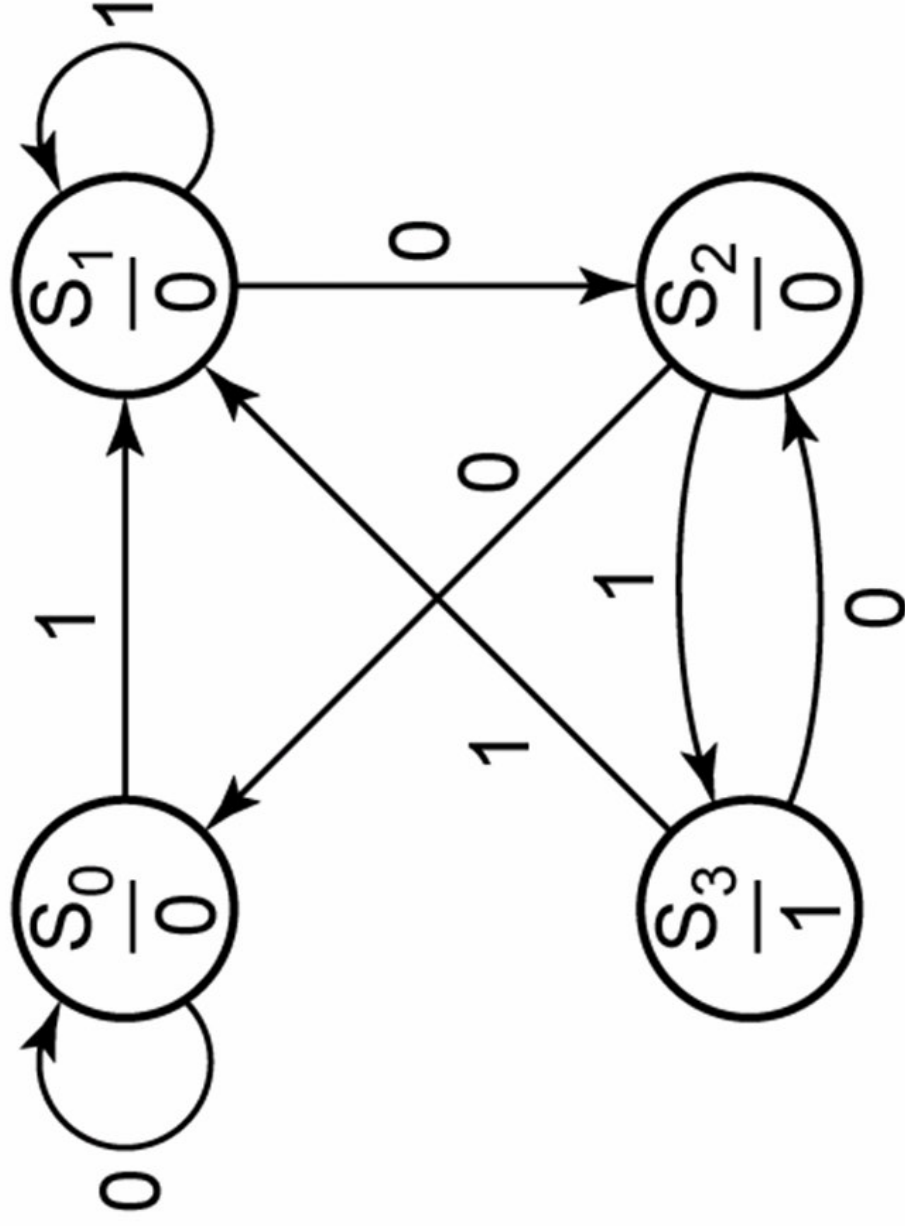


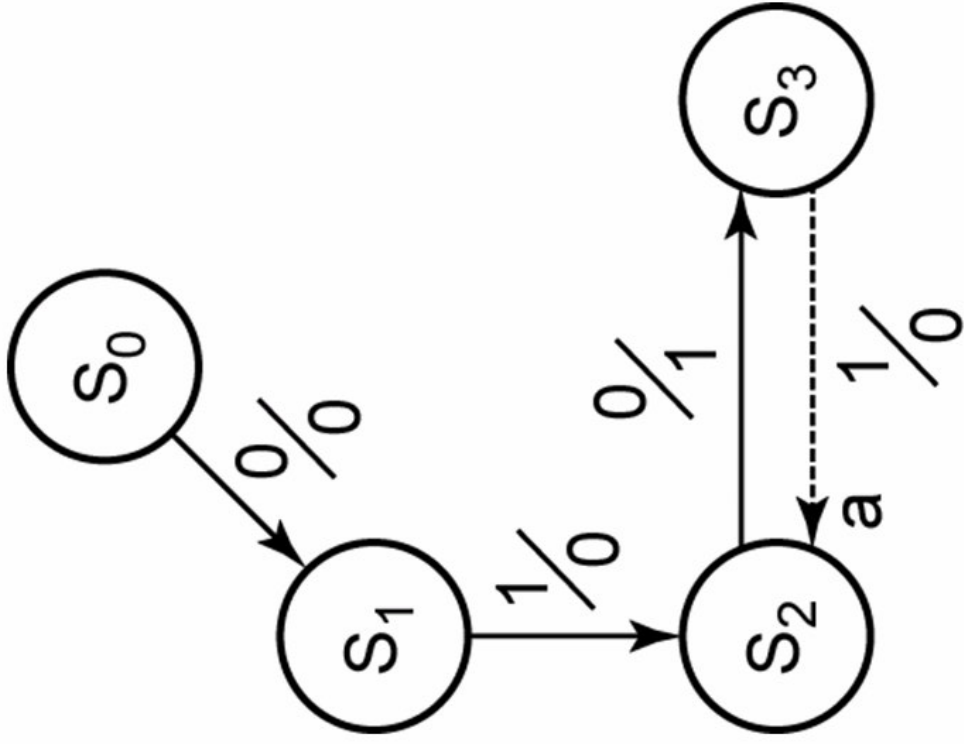
Figure 14-6: Moore State Graph for Sequence Detector

Table 14-3 and Table 14-4

Present State	Next State		Present Output (Z)
	X = 0	X = 1	
S ₀	S ₀	S ₁	0
S ₁	S ₂	S ₁	0
S ₂	S ₀	S ₃	0
S ₃	S ₂	S ₁	1

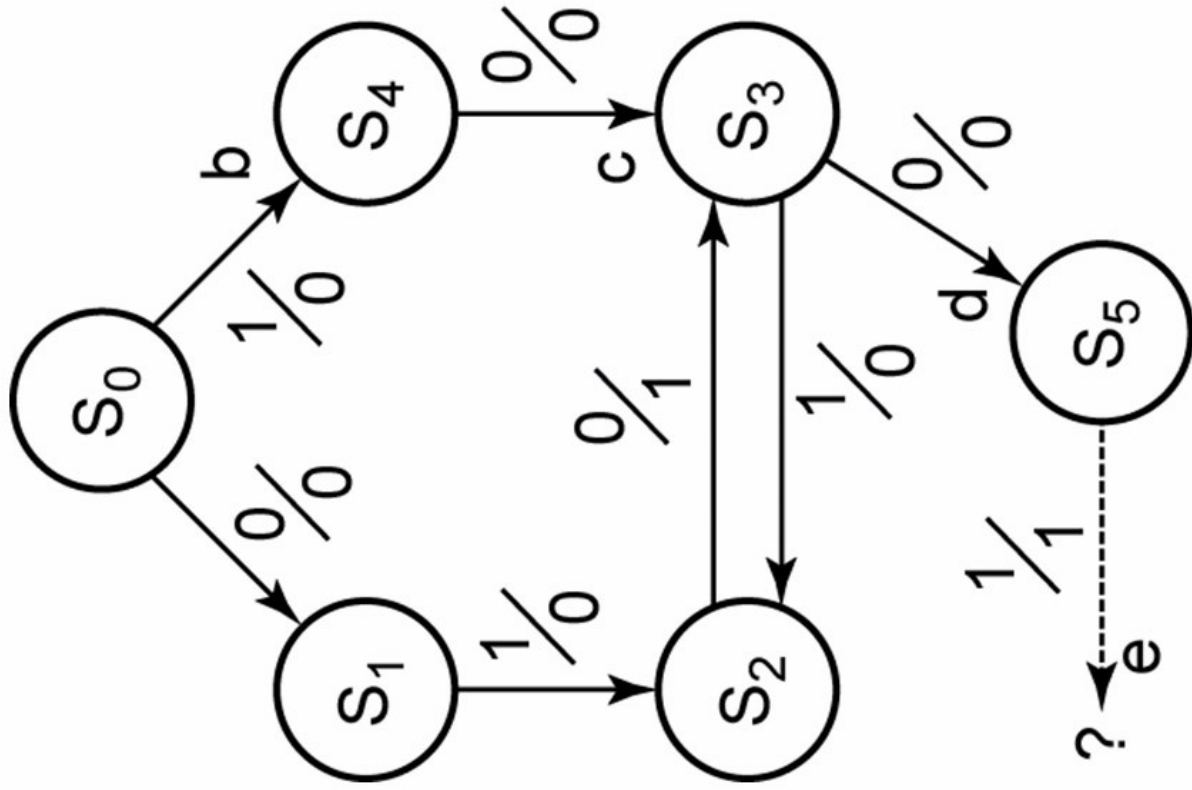
AB	A ⁺ B ⁺		Z
	X = 0	X = 1	
00	00	01	0
01	11	01	0
11	00	10	0
10	11	01	1





<u>state</u>	<u>sequence received</u>
S_0	reset
S_1	0
S_2	01
S_3	010

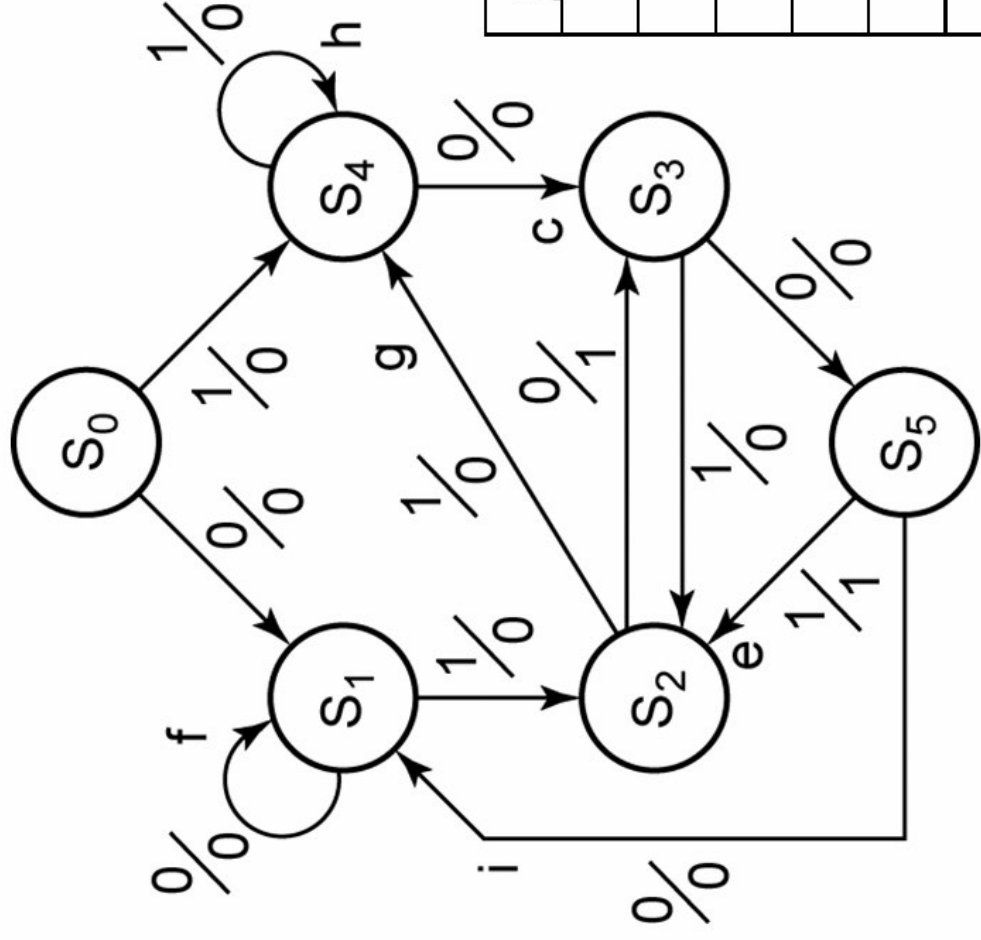
Figure 14-7



<u>state</u>	<u>sequence ends in</u>
S ₀	reset
S ₁	0 (but not 10)
S ₂	01
S ₃	10
S ₄	1 (but not 01)
S ₅	100

Figure 14-8





<u>state</u>	<u>sequence ends in</u>
S ₀	reset
S ₁	0 (but not 10)
S ₂	01
S ₃	10
S ₄	1 (but not 01)
S ₅	100

Figure 14-9

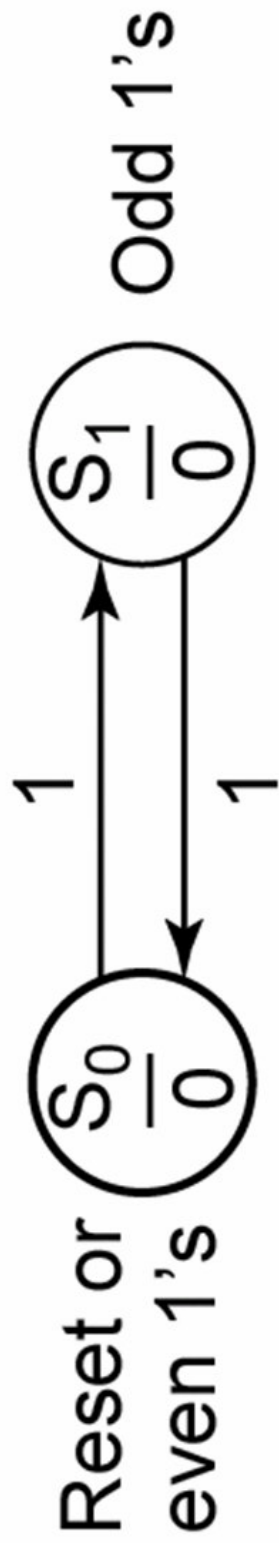
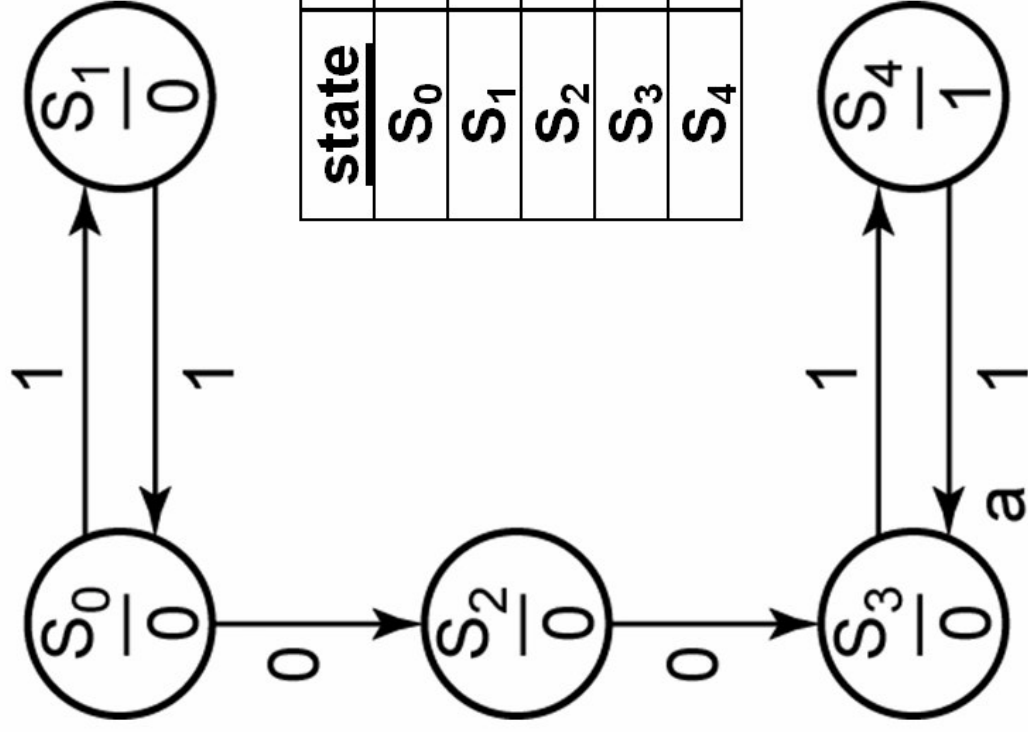
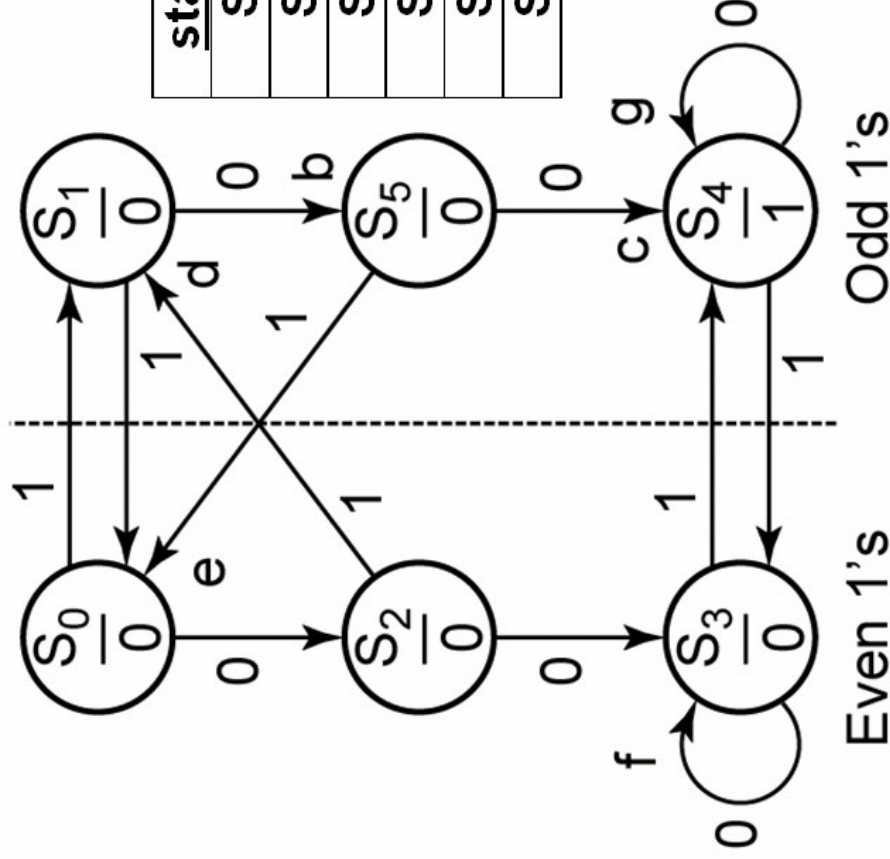


Figure 14-10



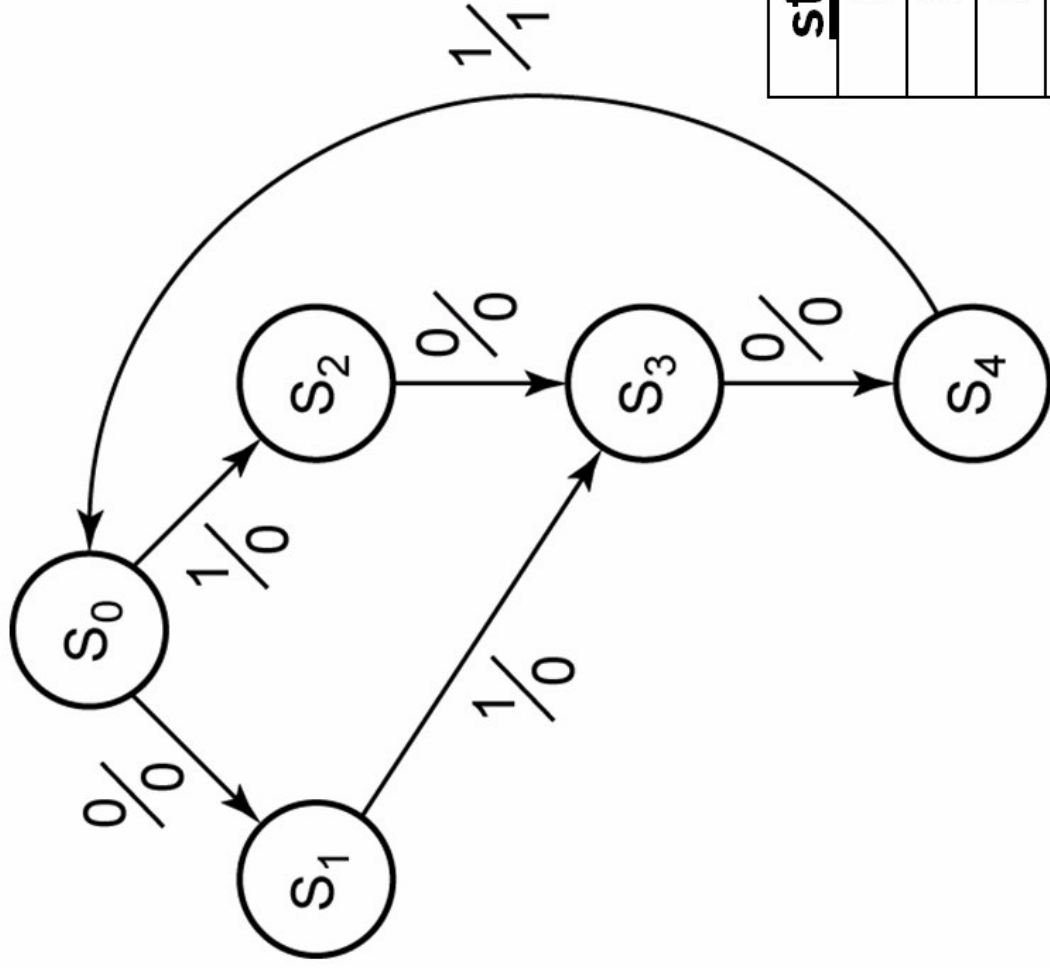
<u>state</u>	<u>sequence received</u>
S ₀	reset or even 1's
S ₁	odd 1's
S ₂	even 1's and ends in 0
S ₃	even 1's and 00 has occurred
S ₄	00 has occurred and odd 1's

Figure 14-11



<u>state</u>	<u>input sequences</u>
S_0	reset or even 1's
S_1	odd 1's
S_2	even 1's and ends in 0
S_3	even 1's and 00 has occurred
S_4	odd 1's and 00 has occurred
S_5	odd 1's and ends in 0

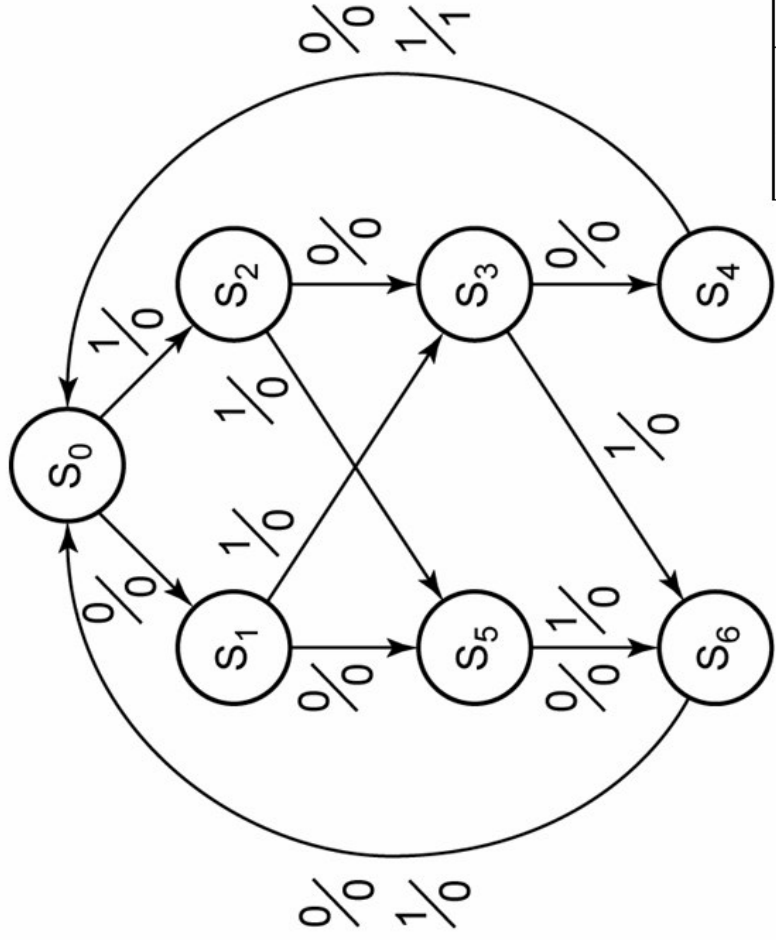
Figure 14-12



<u>state</u>	<u>sequence received</u>
S ₀	reset
S ₁	0
S ₂	1
S ₃	01 or 10
S ₄	010 or 100

Figure 14-13: Partial State Graph for Example 1



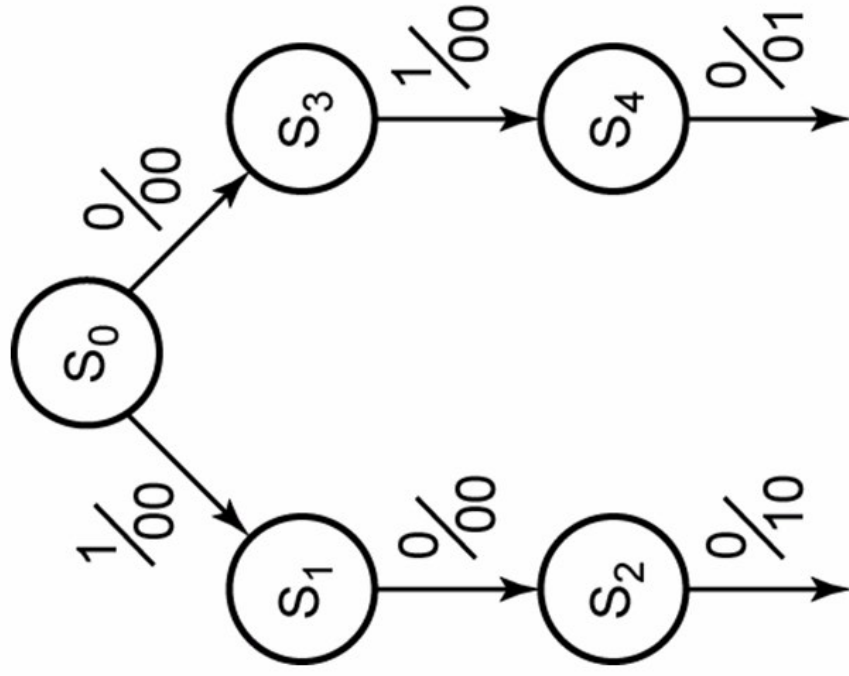


state	sequence received
S ₀	reset
S ₁	0
S ₂	1
S ₃	01 or 10
S ₄	010 or 100
S ₅	2 inputs received, no 1 output is possible
S ₆	3 inputs received, no 1 output is possible

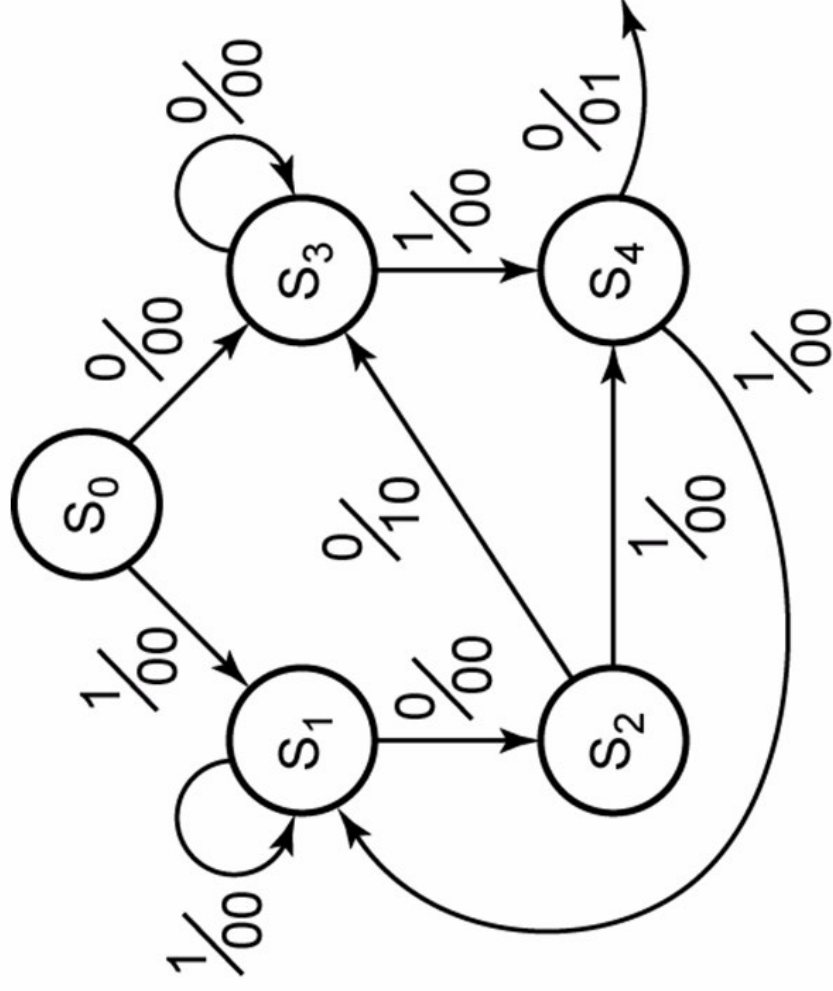
Figure 14-14: Complete State Graph for Example 1

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(a)



(b)

Figure 14-15: Partial Graphs for Example 2

Table 14-5 State Descriptions for Example 2

<u>State</u>	<u>Description</u>
S ₀	No progress on 100
S ₁	Progress of 1 on 100
S ₂	Progress of 10 on 100
S ₃	No progress on 100
S ₄	Progress of 1 on 100
S ₅	No progress on 010
S ₆	Progress of 01 on 010
S ₇	No progress on 010

010 has never occurred

010 has occurred

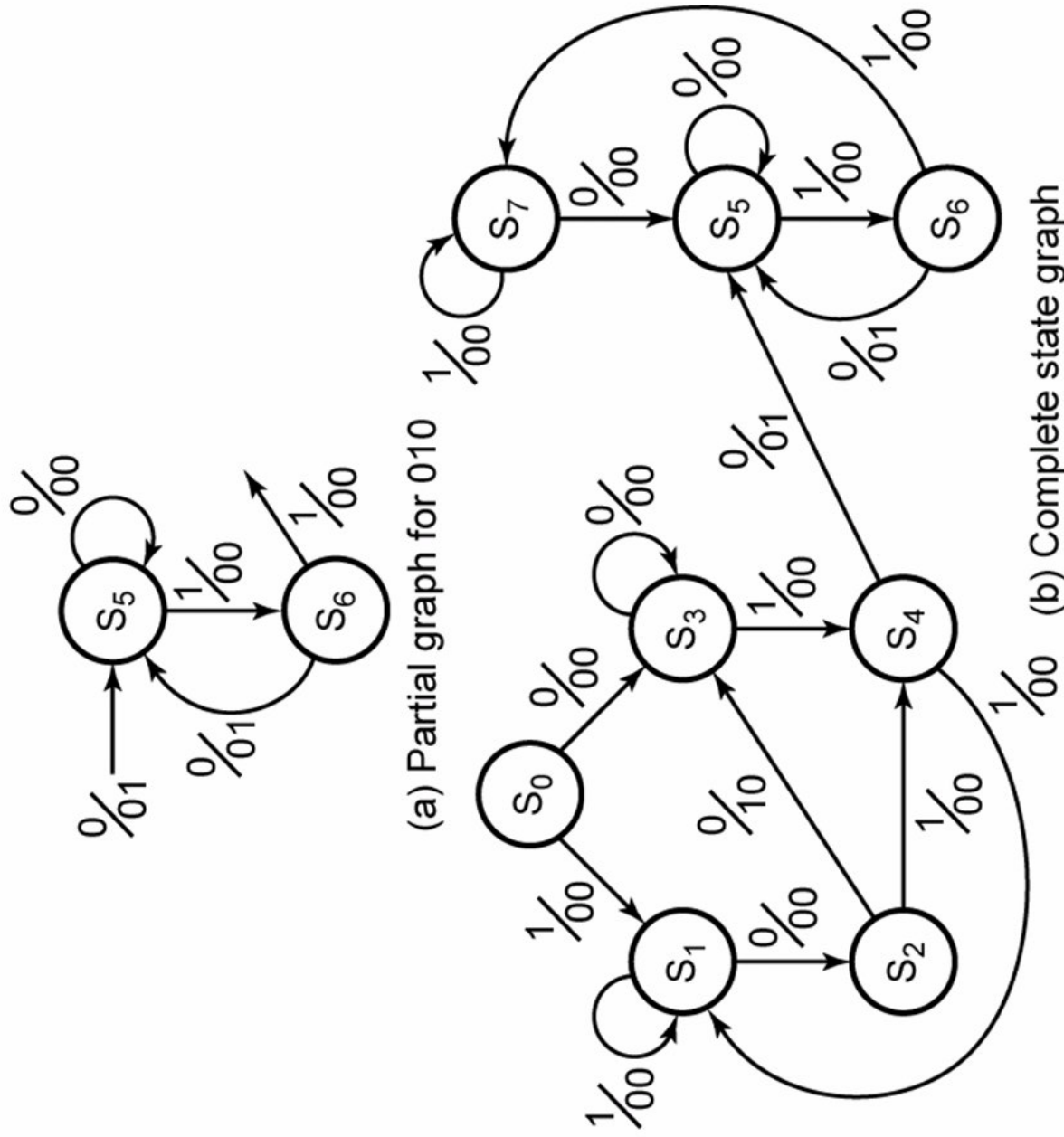


Figure 14-16: State Graphs for Example 2



Table 14-6.

Present State	Next State		Output (Z ₁ Z ₂)	
	X = 0	X = 1	X = 0	X = 1
S ₀	S ₃	S ₁	00	00
S ₁	S ₂	S ₁	00	00
S ₂	S ₃	S ₄	10	00
S ₃	S ₃	S ₄	00	00
S ₄	S ₅	S ₁	01	00
S ₅	S ₅	S ₆	00	00
S ₆	S ₅	S ₇	01	00
S ₇	S ₅	S ₇	00	00



Previous Input (X_1, X_2)	Output (Z)	State Designation
00 or 11	0	S_0
00 or 11	1	S_1
01	0	S_2
01	1	S_3
10	0	S_4
10	1	S_5

Example 3, p. 406



Table 14-7

Present State	Z	Next State			
		$X_1X_2 = 00$	01	11	10
S_0	0	S_0	S_2	S_0	S_4
S_1	1	S_1	S_3	S_1	S_5
S_2	0	S_0	S_2	S_0	S_4
S_3	1	S_1	S_3	S_0	S_5
S_4	0	S_0	S_3	S_1	S_4
S_5	1	S_1	S_2	S_1	S_5

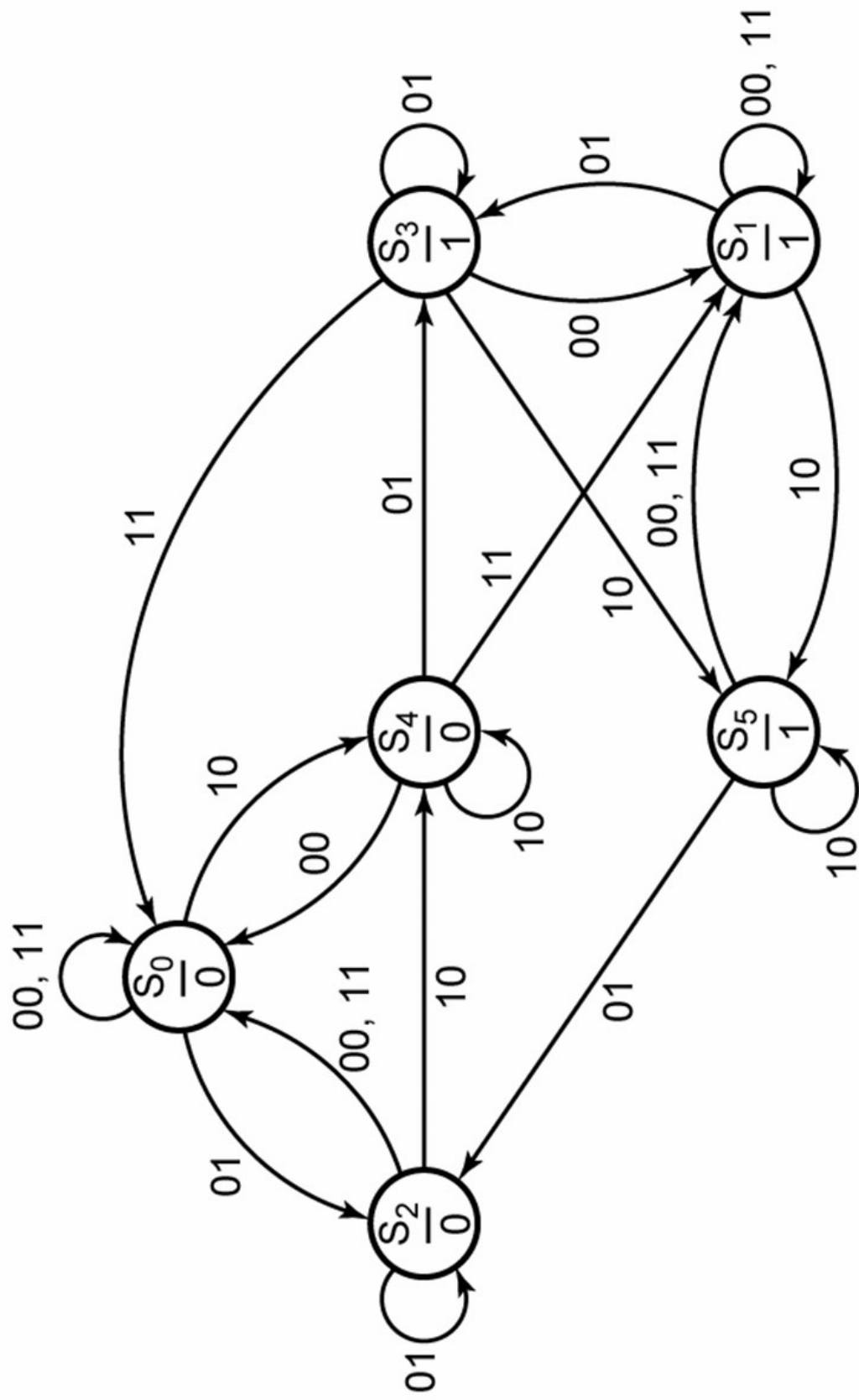
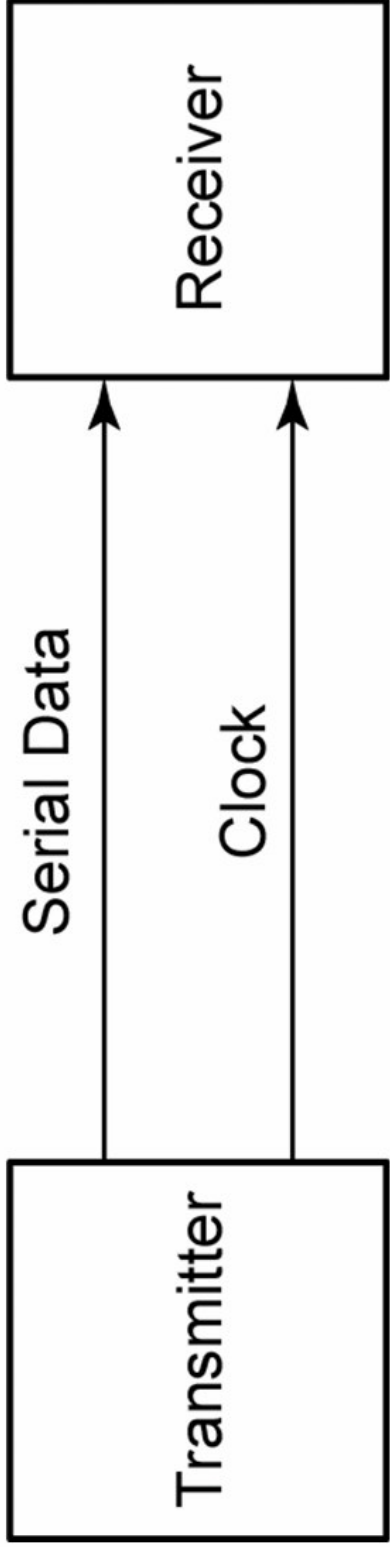
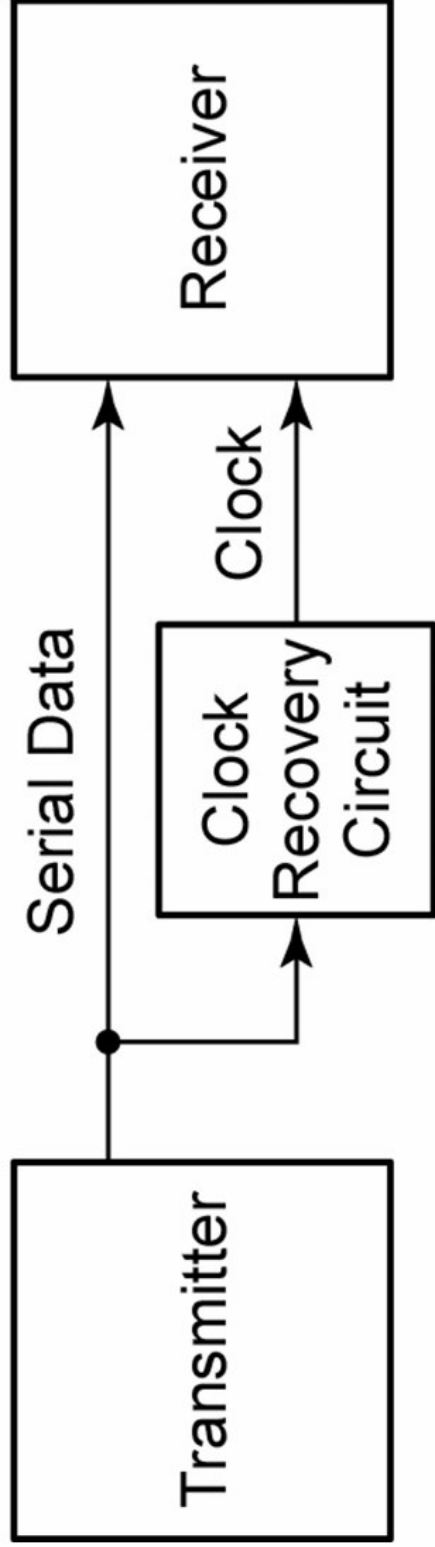


Figure 14-17: State Graph for Example 3



(a)



(b)

Figure 14-18: Serial Data Transmission

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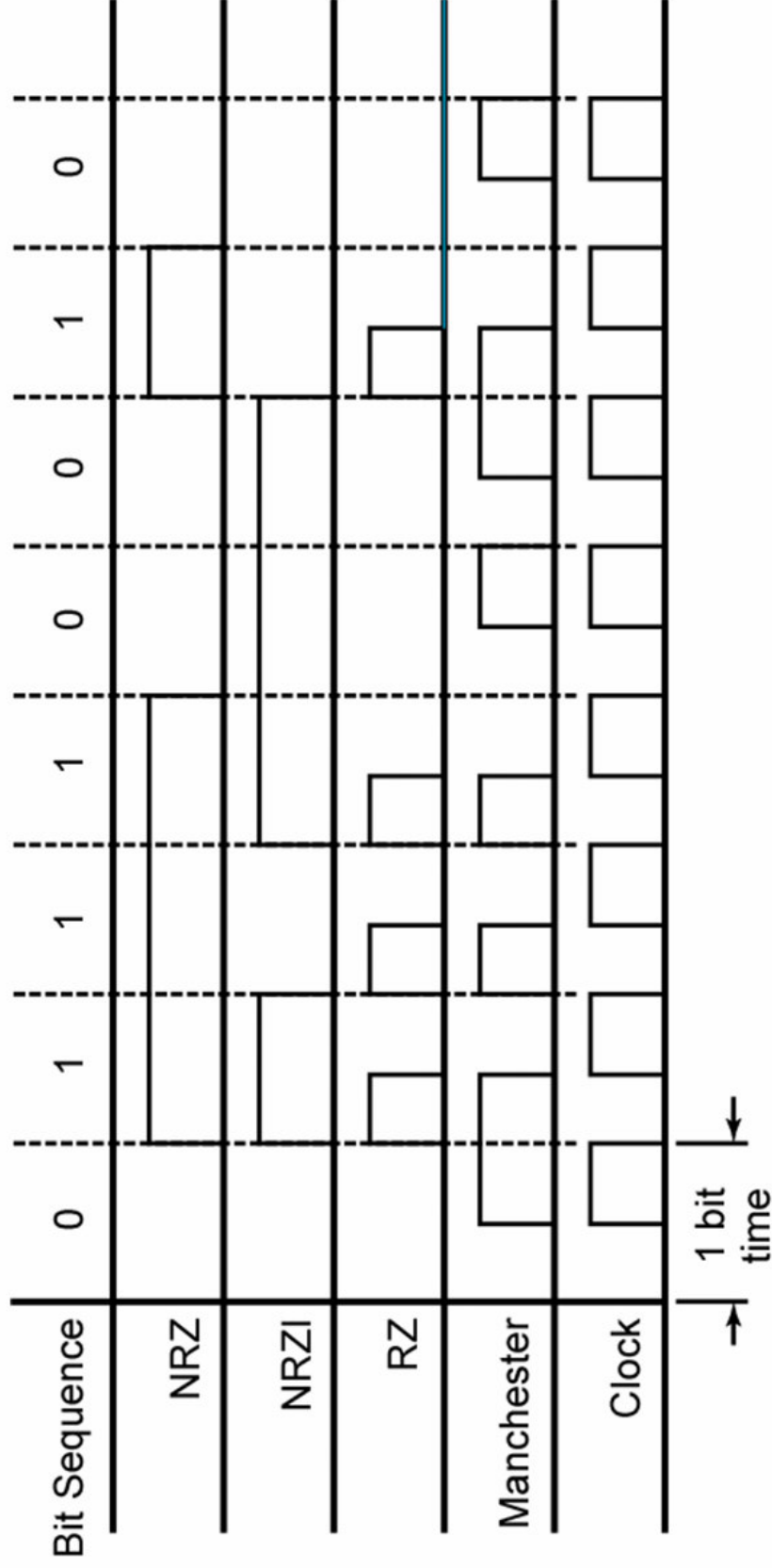


Figure 14-19: Coding Schemes for Serial Data Transmission



(a) Conversion network

Figure 14-20a:
Mealy Circuit for NRZ-to-Manchester Conversion

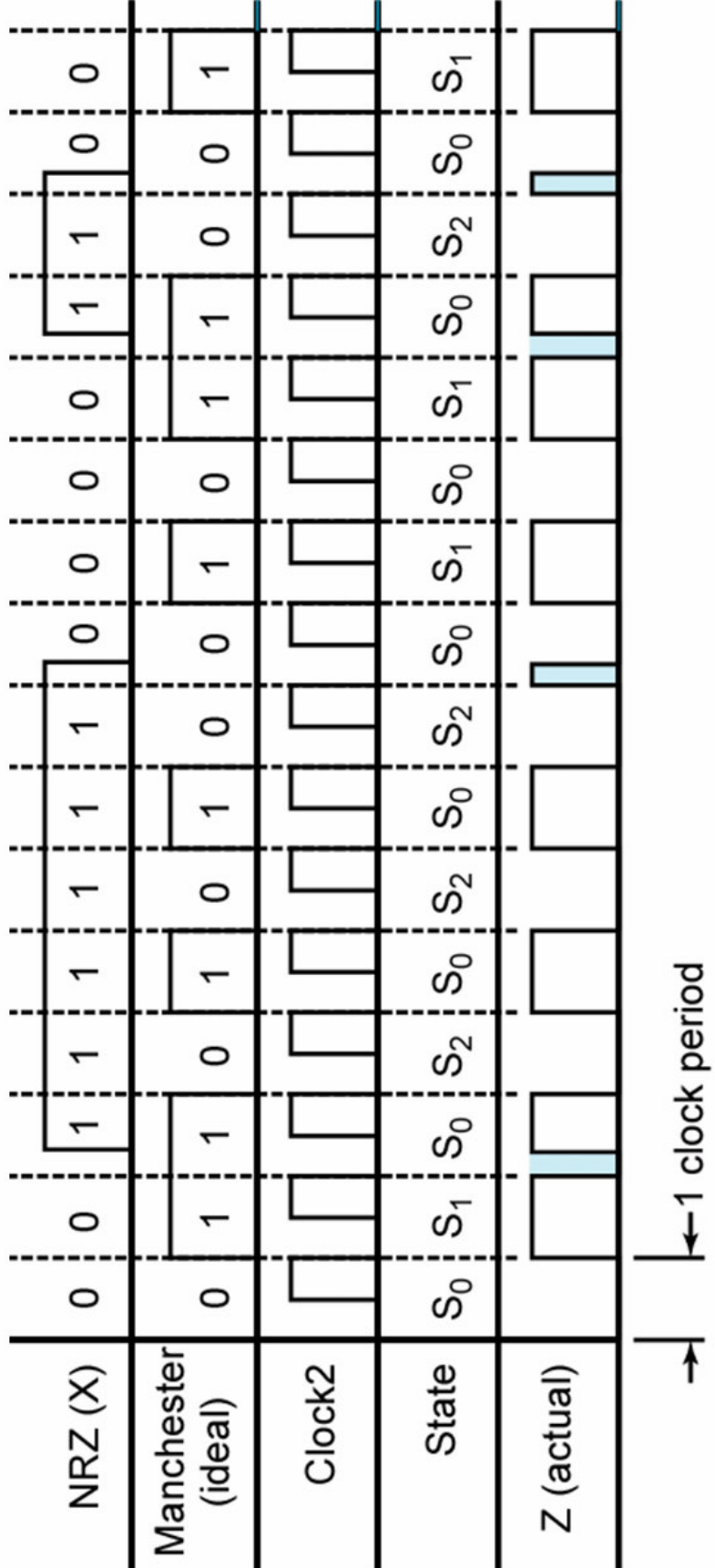
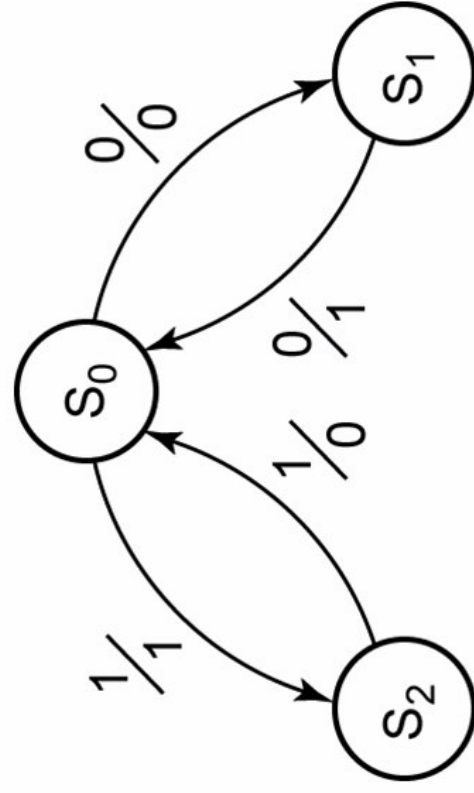


Figure 14-20b:
Mealy Circuit for NRZ-to-Manchester Conversion

Present State	Next State		Output (Z)	
	X = 0	X = 1	X = 0	X = 1
S ₀	S ₁	S ₂	0	1
S ₁	S ₀	-	1	-
S ₂	-	S ₀	-	0



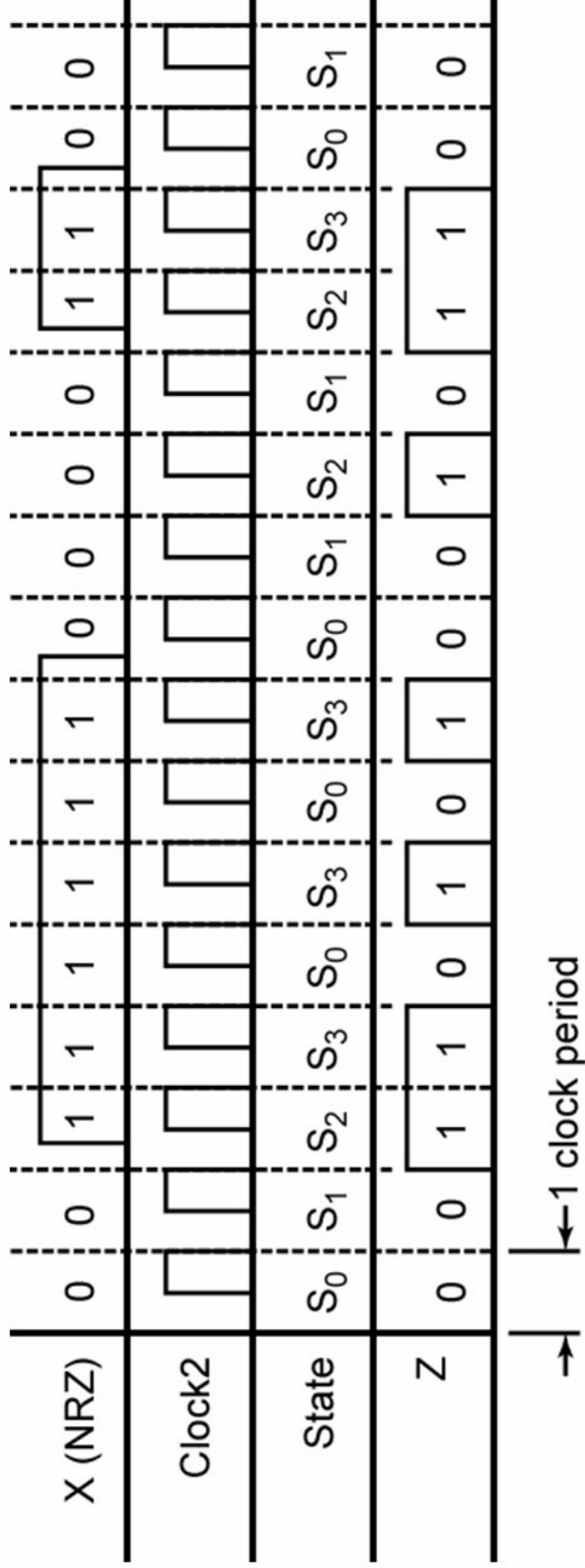
(c) State graph

(d) State table

Figure 14-20cd:

Mealy Circuit for NRZ-to-Manchester Conversion





(a) Timing chart

Figure 14-21a:
Moore Circuit for NRZ-to-Manchester Conversion

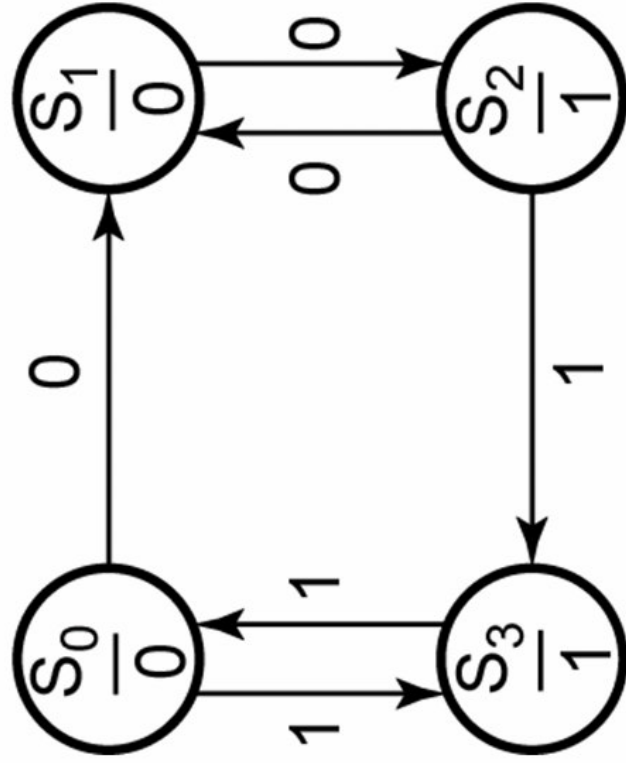


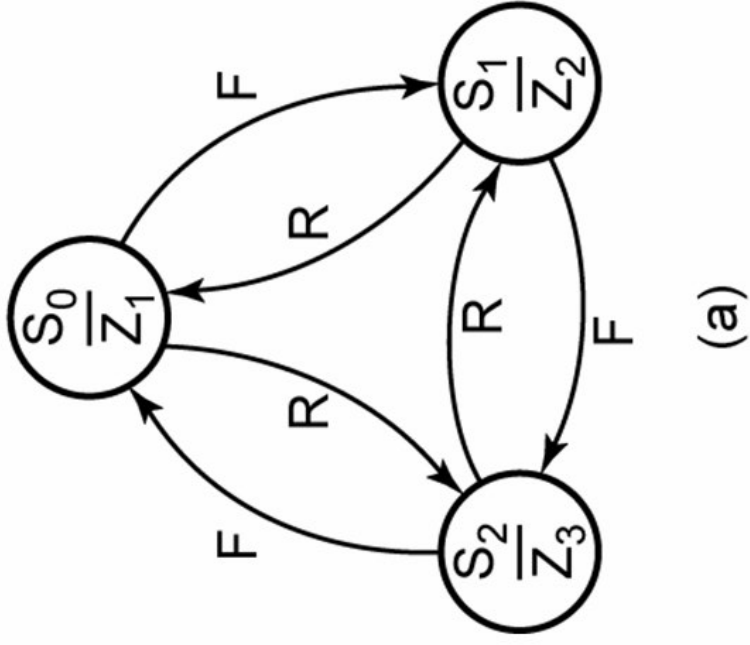
Figure 14-21b:
Moore Circuit for
NRZ-to-Manchester
Conversion

(b) State graph

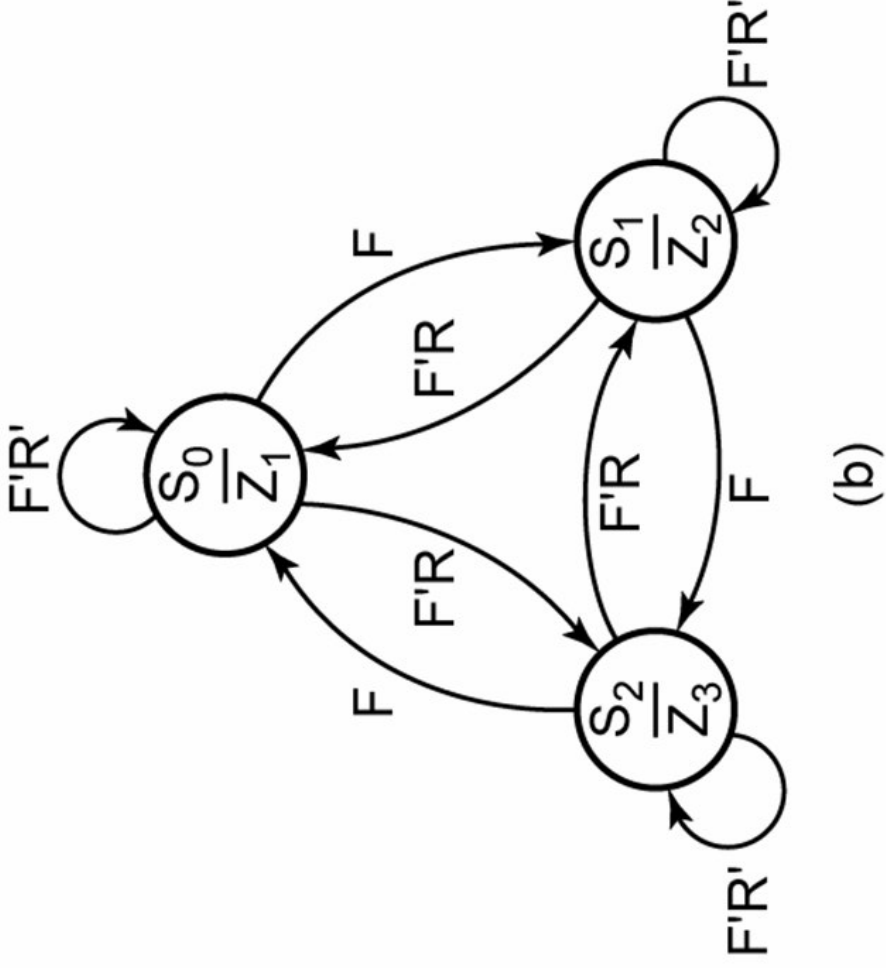
Present State	Next State		Present Output (Z)
	X = 0	X = 1	
S ₀	S ₁	S ₃	0
S ₁	S ₂	-	0
S ₂	S ₁	S ₃	1
S ₃	-	S ₀	1

(c) State table





(a)



(b)

Figure 14-22: State Graphs with Variable Names on Arc Labels

Table 14-8. State Table for Figure 14-22

PS	NS		Output
FR=00	01	10	Z₁Z₂Z₃
S₀	S₂	S₁	1 0 0
S₁	S₀	S₂	0 1 0
S₂	S₁	S₀	0 0 1