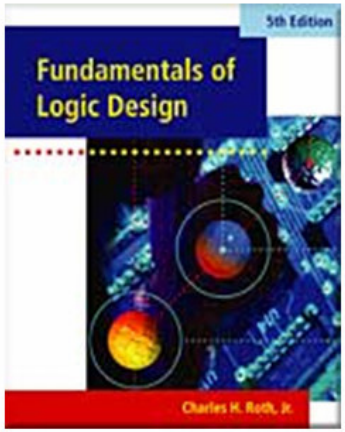
FIGURES FOR

CHAPTER 13

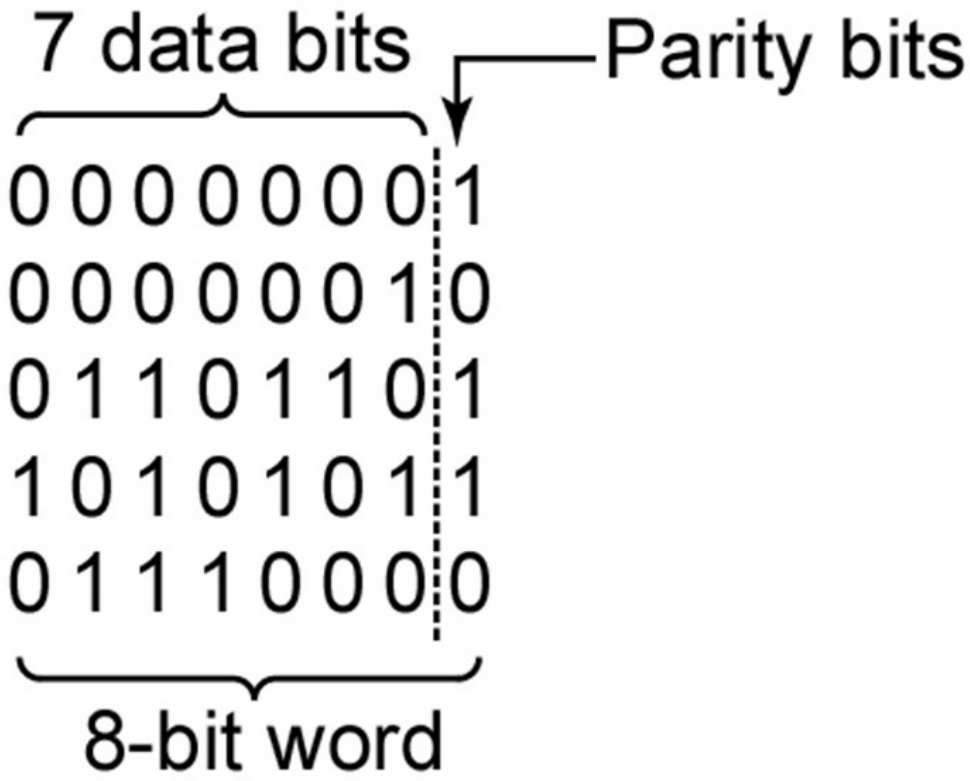
ANALYSIS OF CLOCKED SEQUENTIAL CIRCUITS



This chapter in the book includes:

Objectives
Study Guide
13.1 A Sequential Parity Checker
13.2 Analysis by Signal Tracing and Timing Charts
13.3 State Tables and Graphs
13.4 General Models for Sequential Circuits
Programmed Exercise
Problems

Click the mouse to move to the next page.
Use the ESC key to exit this chapter.



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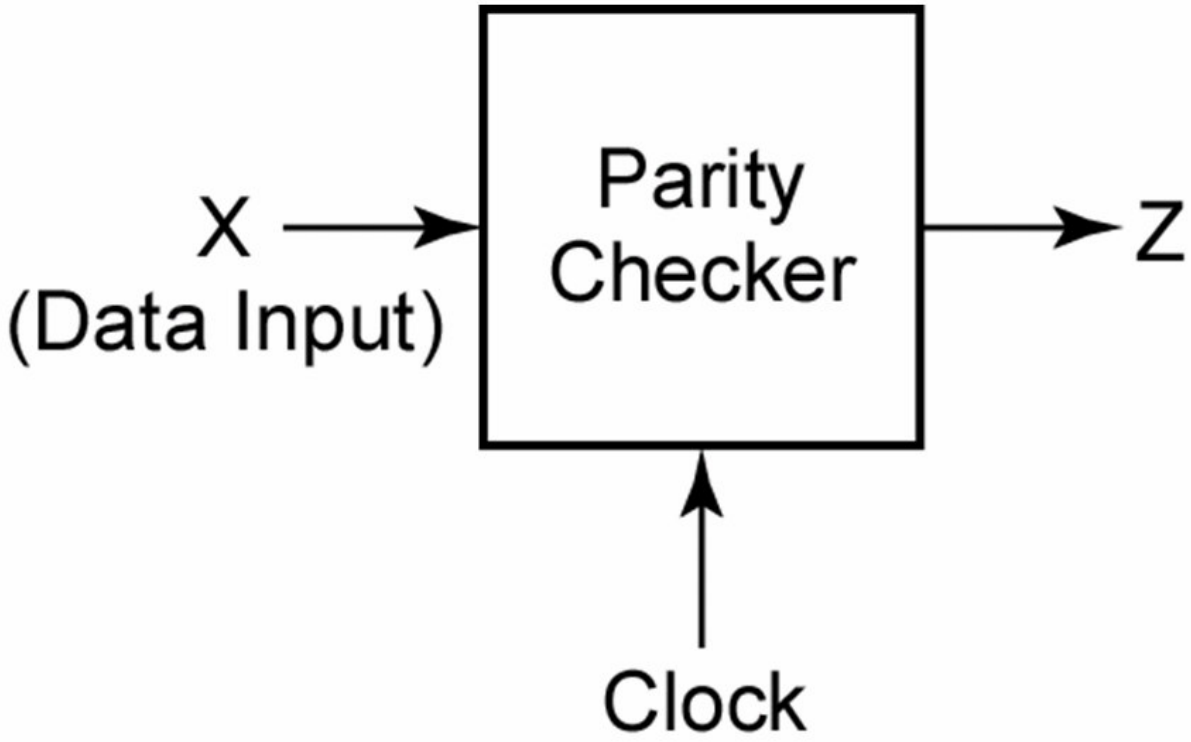

Figure 13-1: **Block Diagram for Parity Checker**

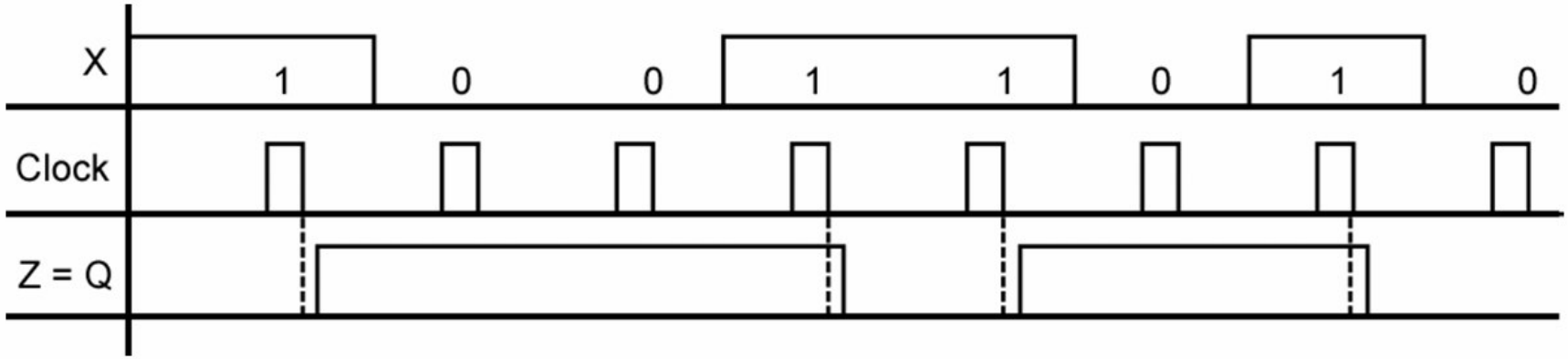

Figure 13-2: **Waveforms for Parity Checker**

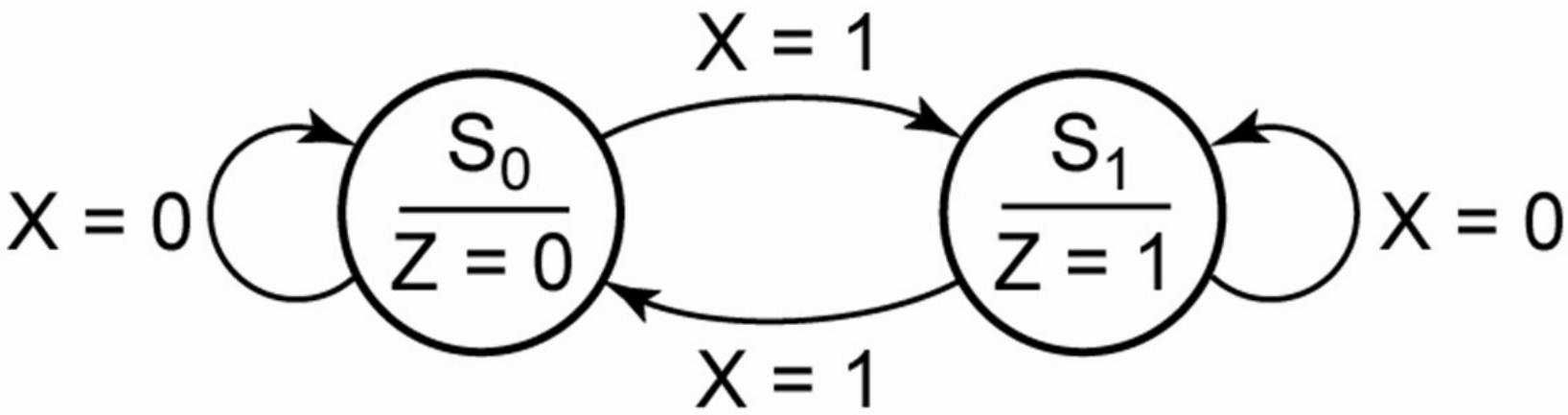

Figure 13-3: **State Graph for Parity Checker**

Table 13-1: State Table for Parity Checker

(a)

Present State	Next State $X = 0$	Next State $X = 1$	Present Output
S_0	S_0	S_1	0
S_1	S_1	S_0	1

(b)

	Q^+		T		
Q	$X = 0$	$X = 1$	$X = 0$	$X = 1$	Z
0	0	1	0	1	0
1	1	0	0	1	1

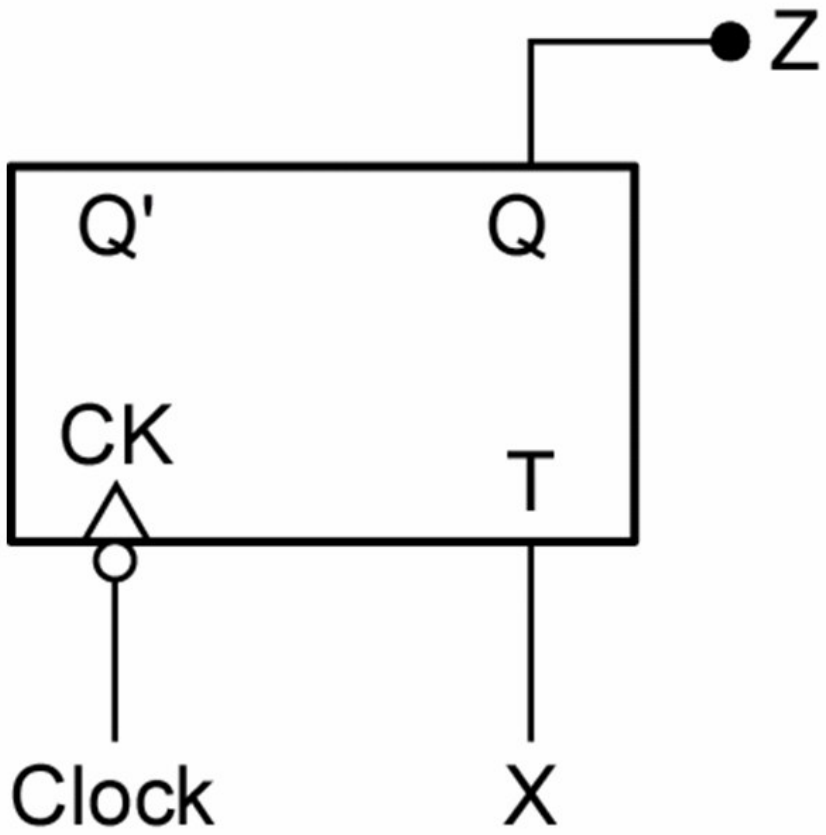

Figure 13-4: **Parity Checker**

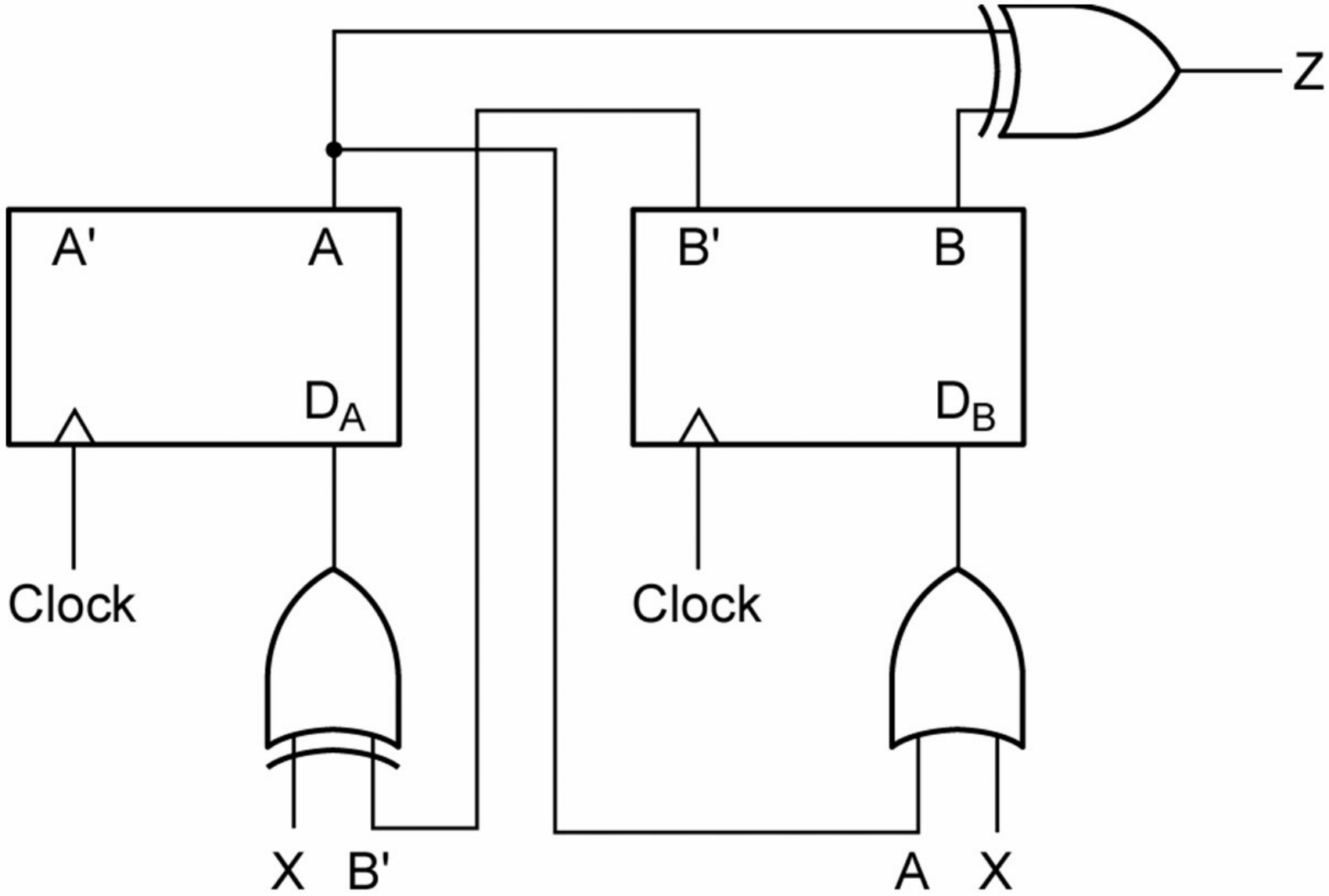

Figure 13-5: **Moore Sequential Circuit to be Analyzed**

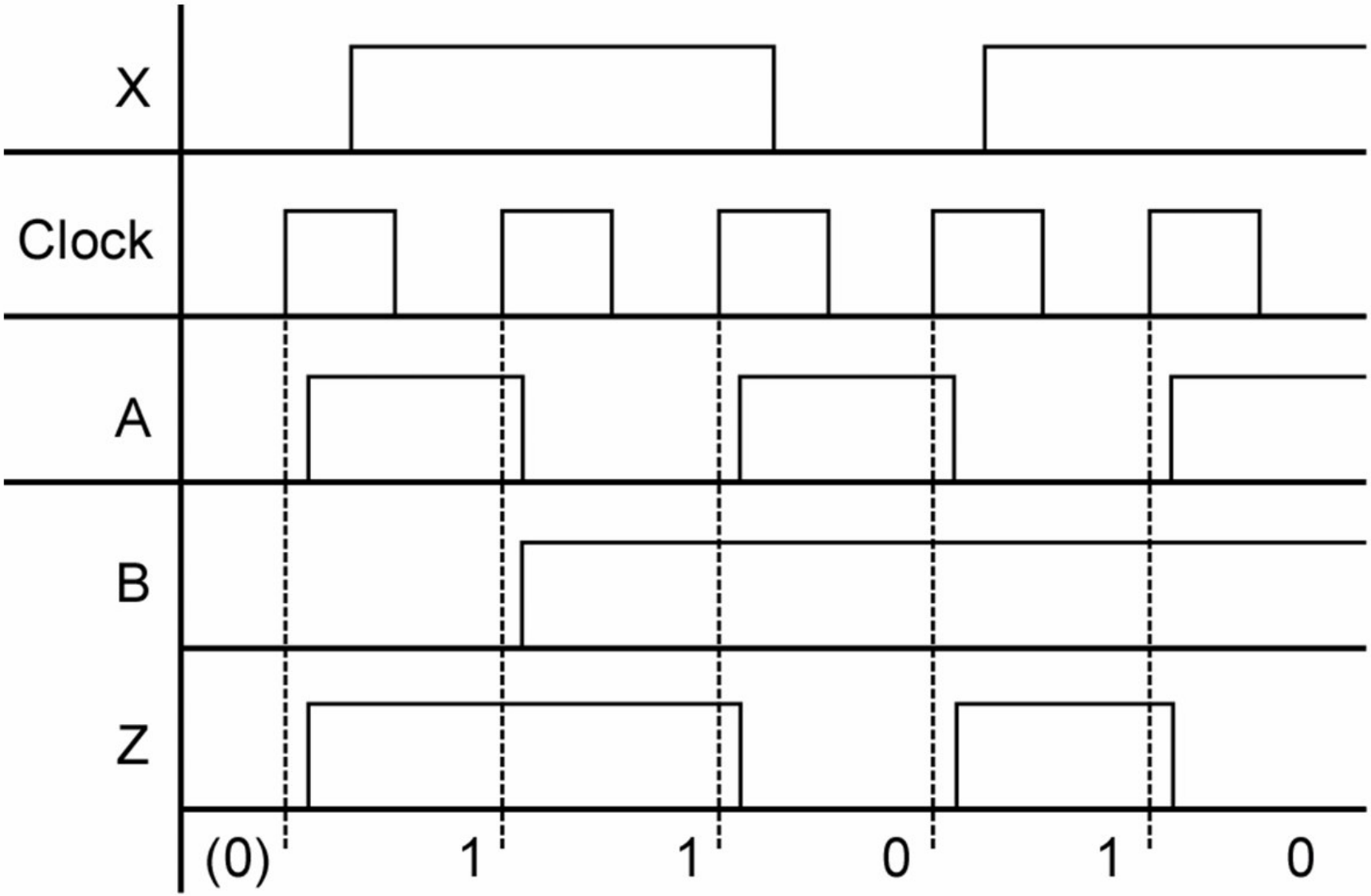

Figure 13-6: **Timing Chart for Figure 13-5**

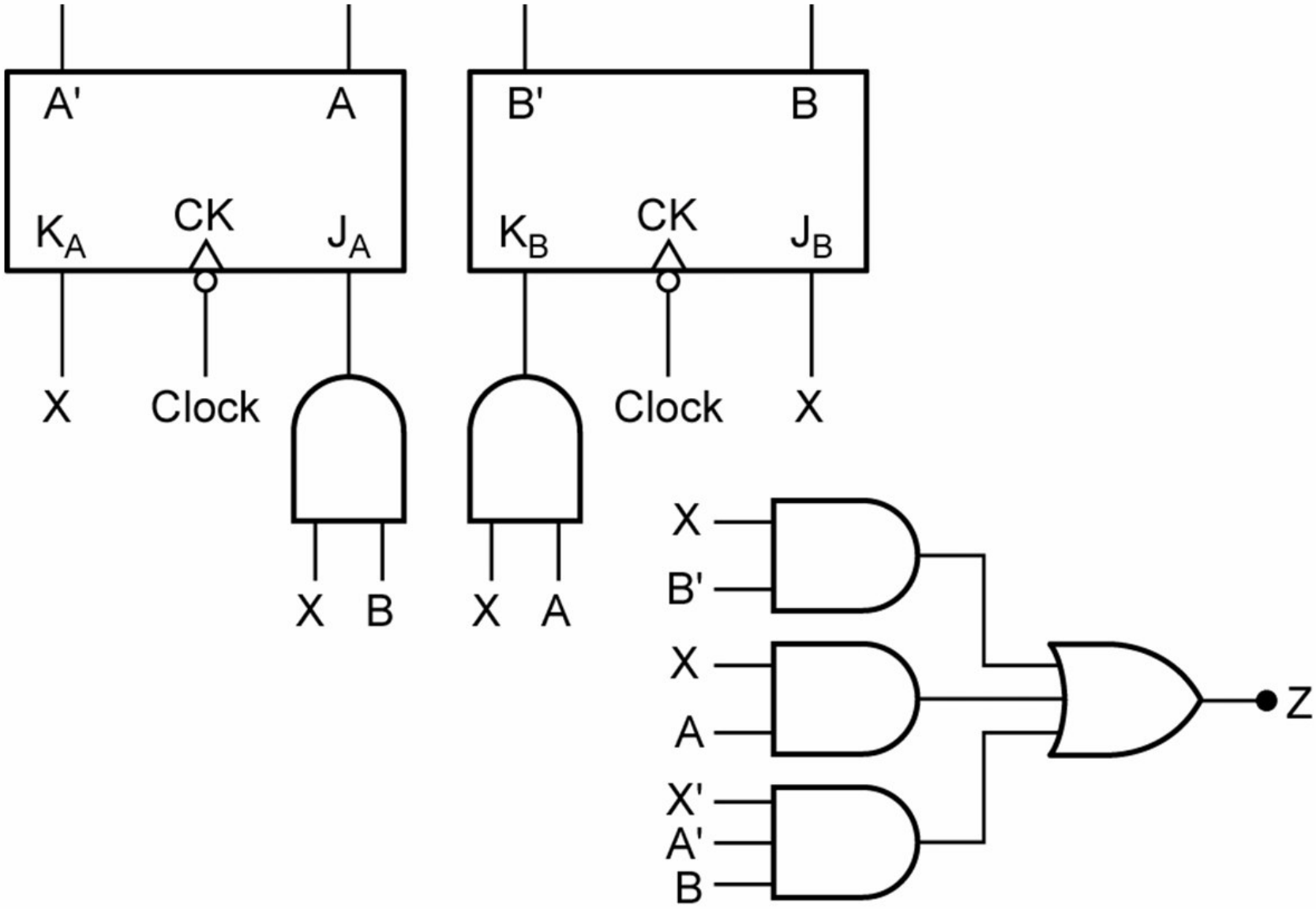

Figure 13-7: **Mealy Sequential Circuit to be Analyzed**

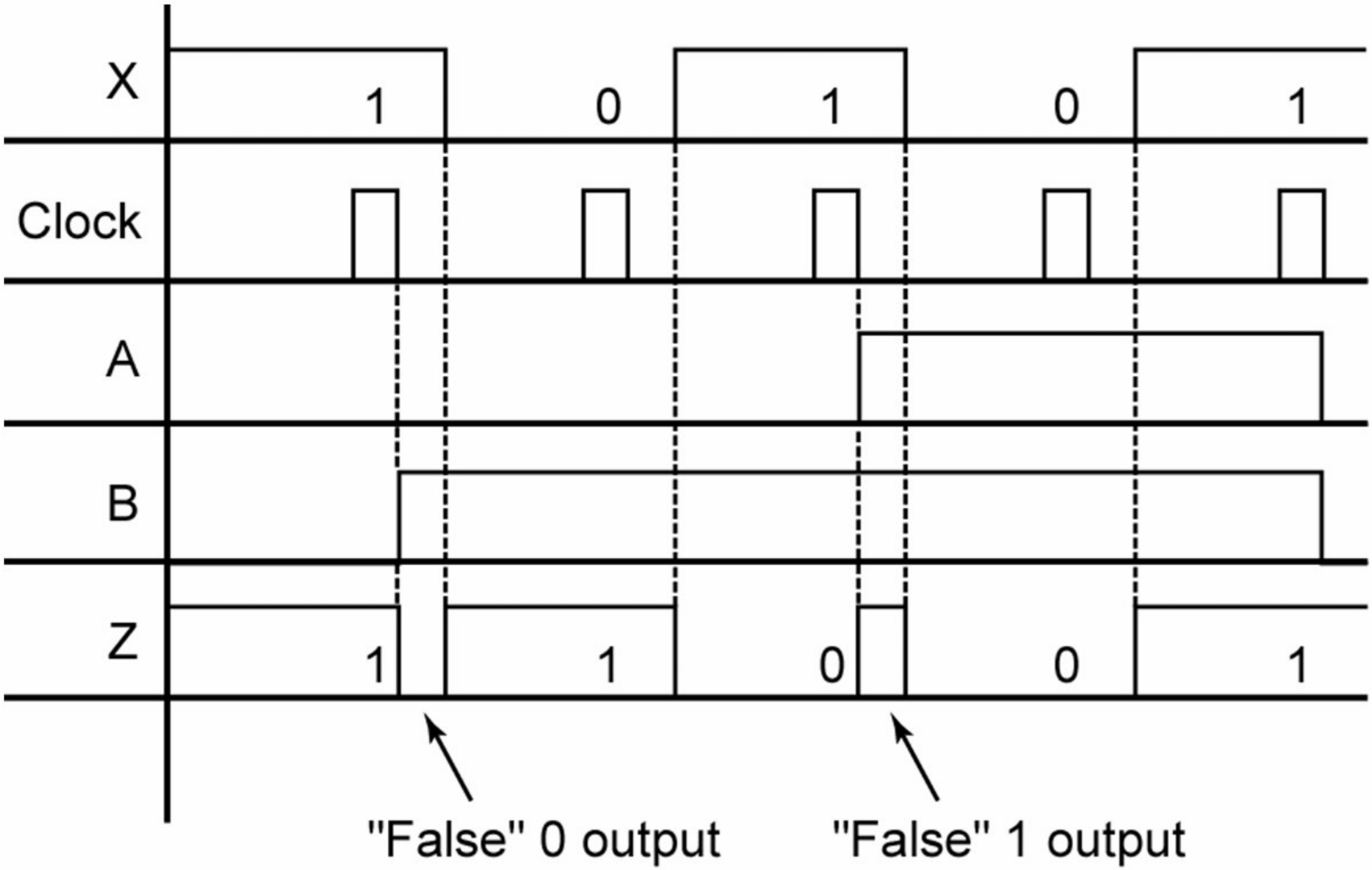

Figure 13-8: **Timing Chart for Circuit of Figure 13-7**

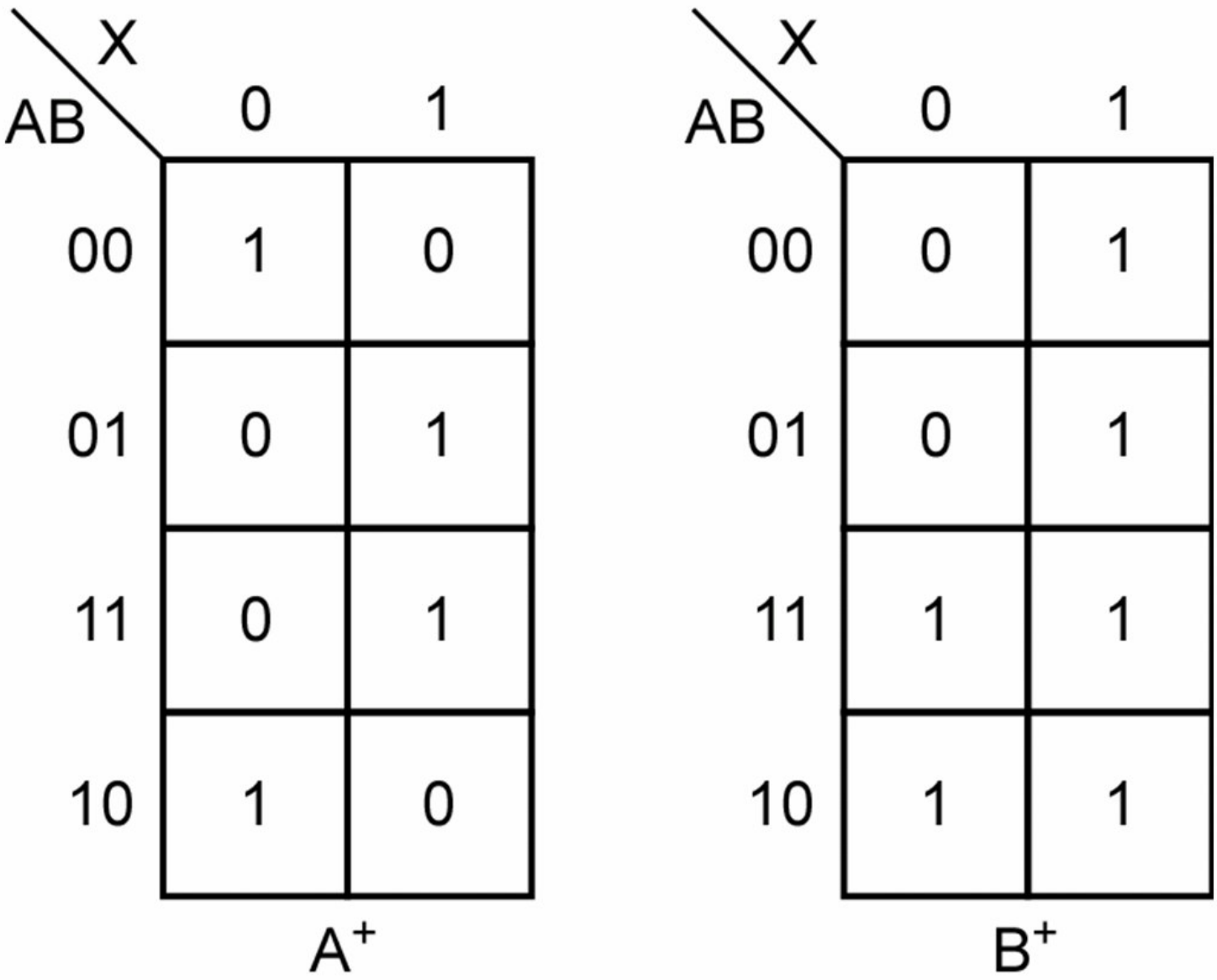

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Table 13-2. Moore State Tables for Figure 13-5

(a)

AB	A^+B^+ X=0	A^+B^+ X=1	Z
00	10	01	0
01	00	11	1
11	01	11	0
10	11	01	1

(b)

Present State	Next State X = 0	Next State X = 1	Present Output(Z)
S_0	S_3	S_1	0
S_1	S_0	S_2	1
S_2	S_1	S_2	0
S_3	S_2	S_1	1

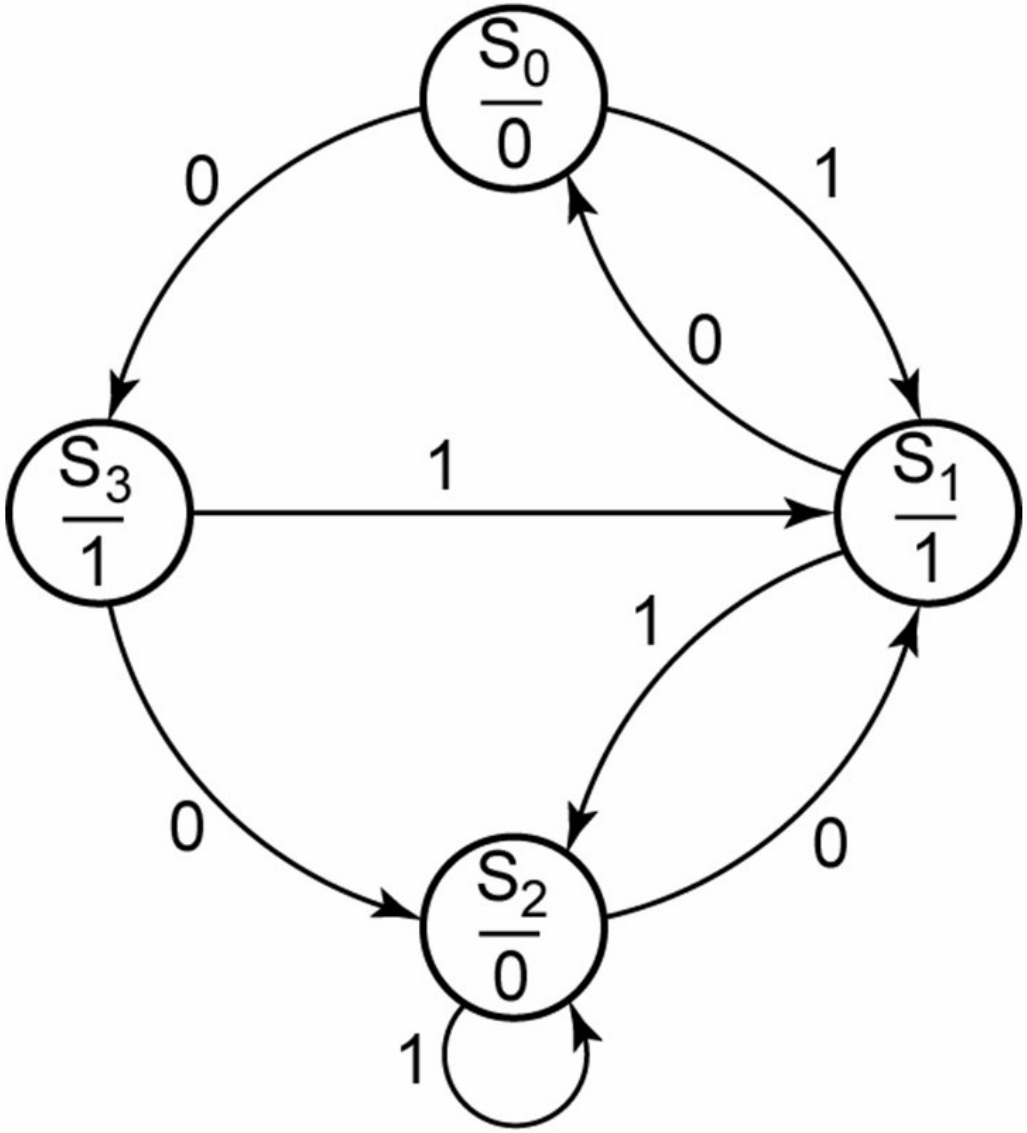
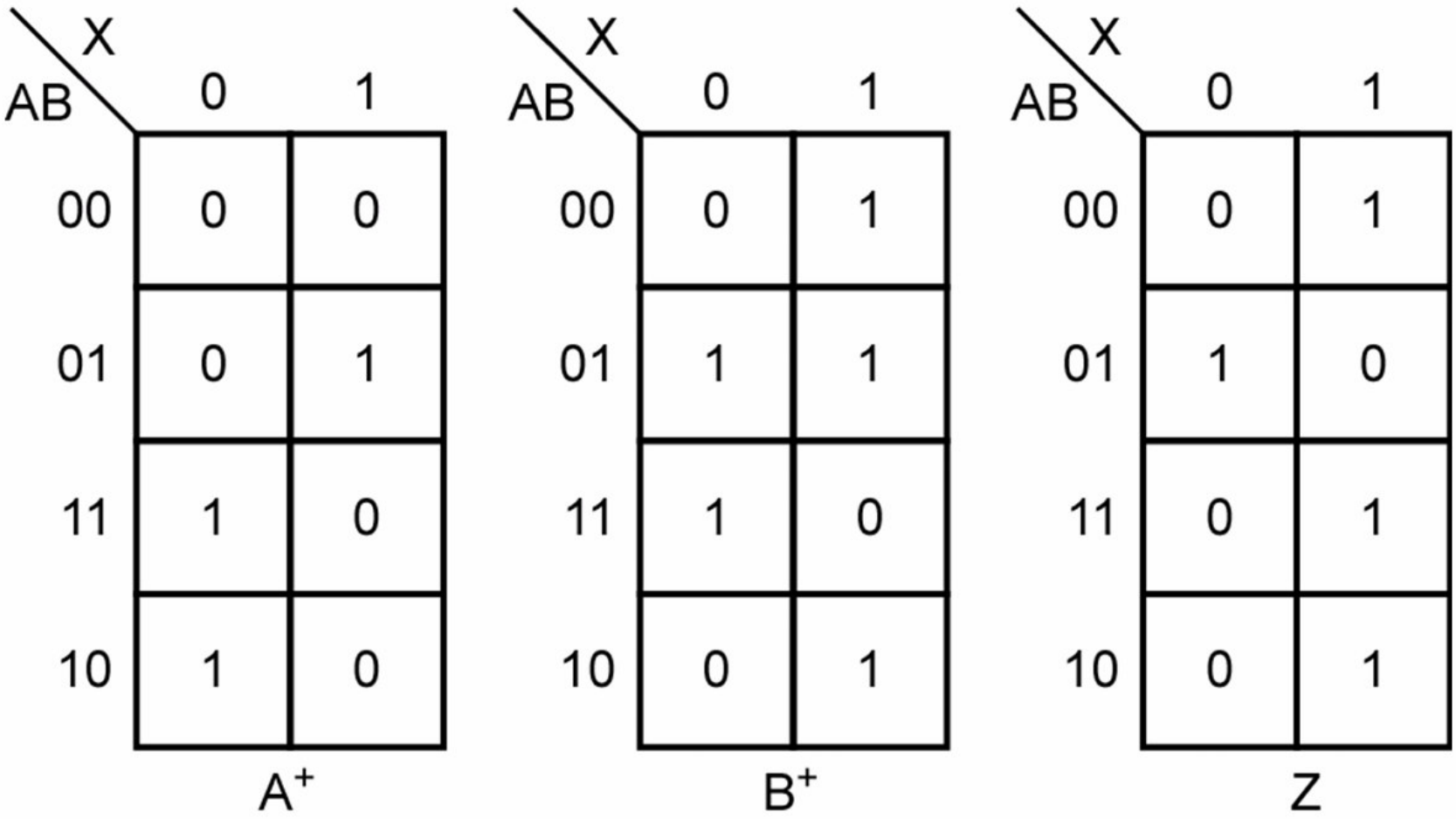


Figure 13-9: **Moore State Graph for Figure 13-5**



AB \ X	0	1
00	0	0
01	0	1
11	1	0
10	1	0

A^+

AB \ X	0	1
00	0	1
01	1	1
11	1	0
10	0	1

B^+

AB \ X	0	1
00	0	1
01	1	0
11	0	1
10	0	1

Z

Figure 13-10

Table 13-3. Mealy State Tables for Figure 13-7

(a)

	A^+B^+		Z	
AB	$X=0$	1	$X=0$	1
00	00	01	0	1
01	01	11	1	0
11	11	00	0	1
10	10	01	0	1

(b)

Present State	Next State		Present Output	
	$X=0$	1	$X=0$	1
S_0	S_0	S_1	0	1
S_1	S_1	S_2	1	0
S_2	S_2	S_0	0	1
S_3	S_3	S_1	0	1

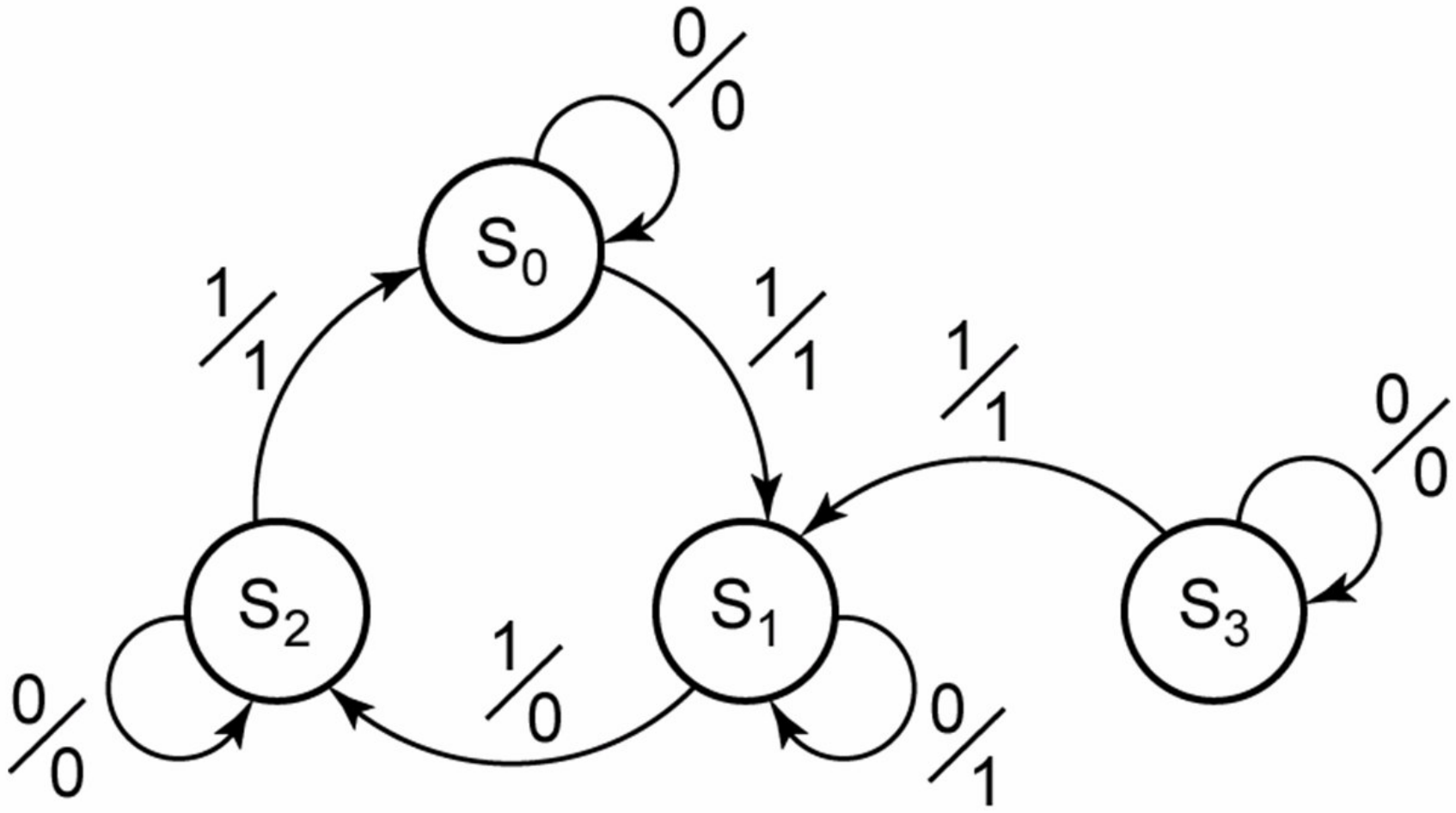
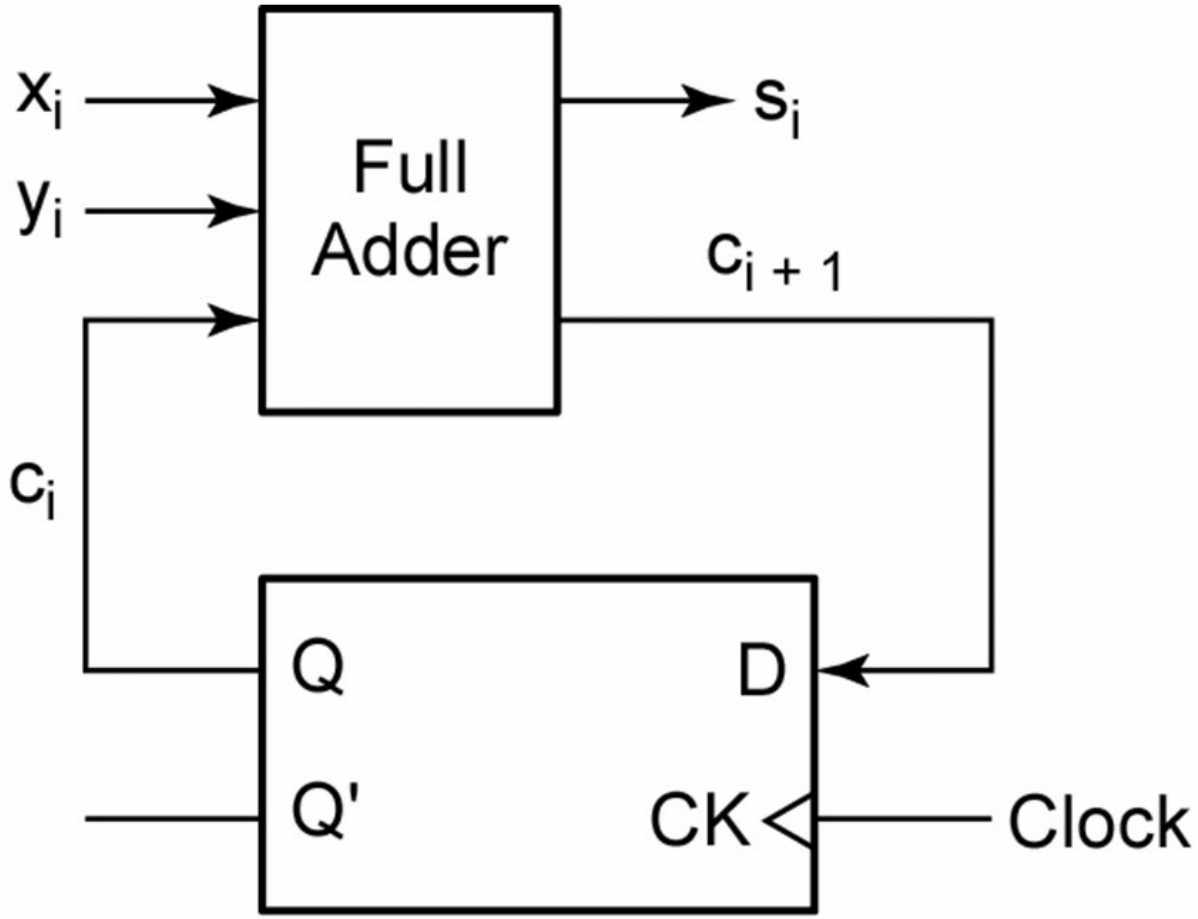


Figure 13-11: **Mealy State Graph for Figure 13-7**



(a) With D flip-flop

Figure 13-12a: **Serial Adder**

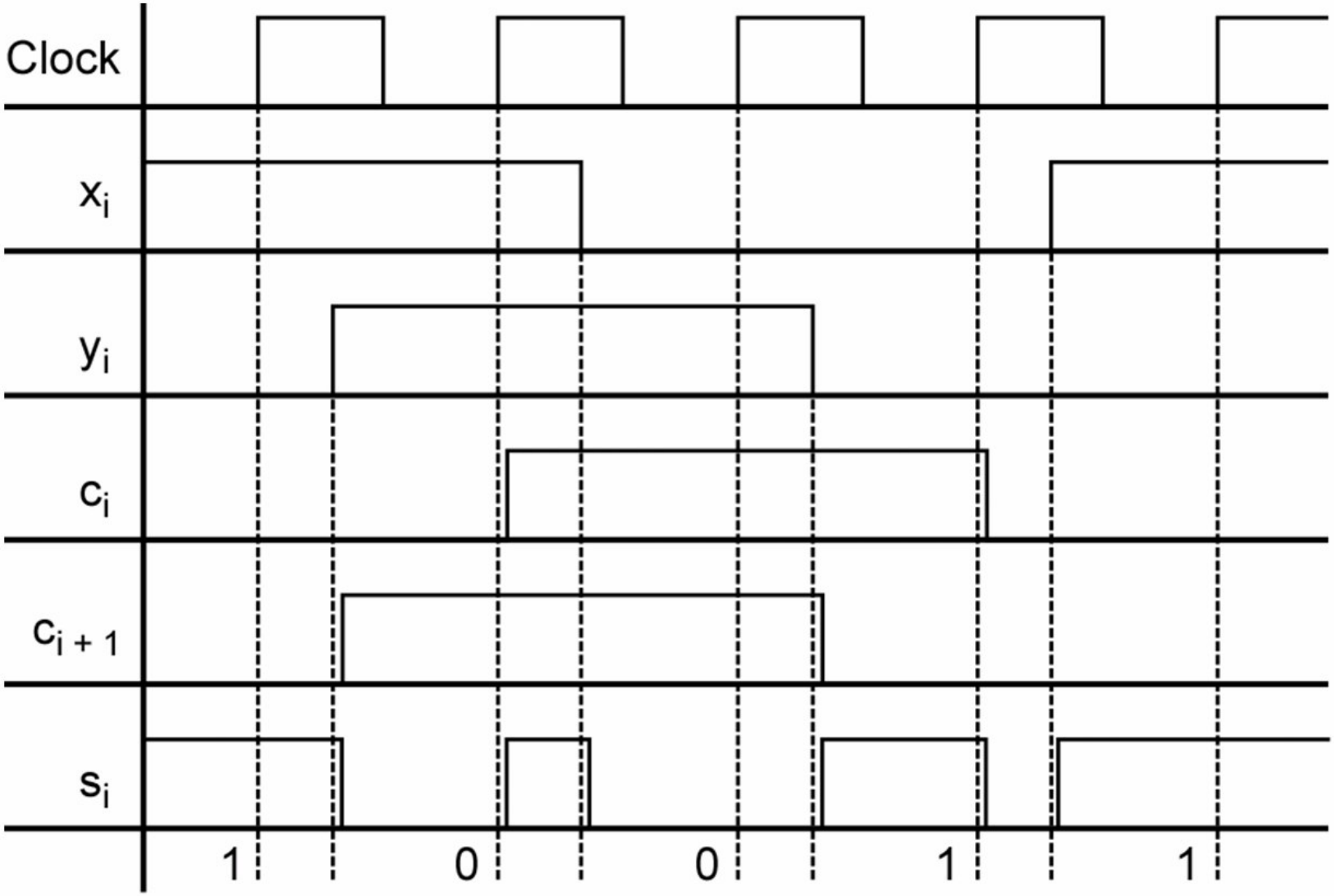


Figure 13-13: **Timing Diagram for Serial Adder**

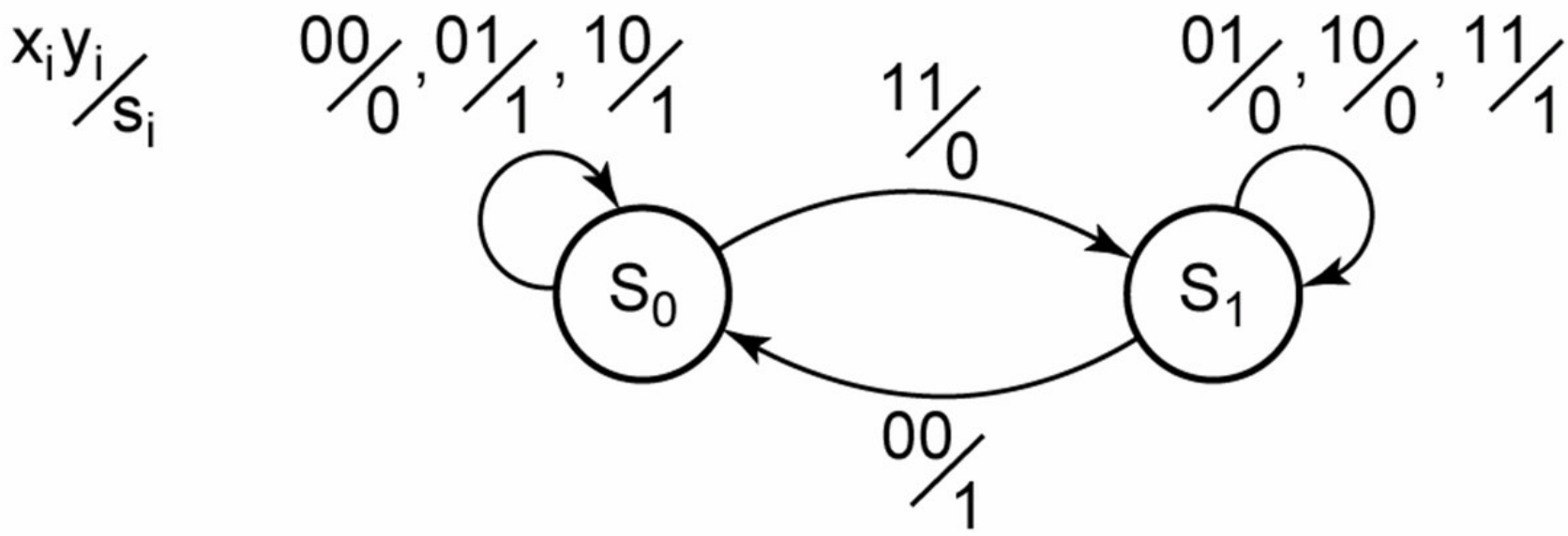


Figure 13-14: **State Graph for Serial Adder**

Table 13-4. A State Table with Multiple Inputs and Outputs

Present State	Next State				Present Output (Z_1Z_2)			
	$X_1X_2 = 00$	01	10	11	$X_1X_2 = 00$	01	10	11
S_0	S_3	S_2	S_1	S_0	00	10	11	01
S_1	S_0	S_1	S_2	S_3	10	10	11	11
S_2	S_3	S_0	S_1	S_1	00	10	11	01
S_3	S_2	S_2	S_1	S_0	00	00	01	01

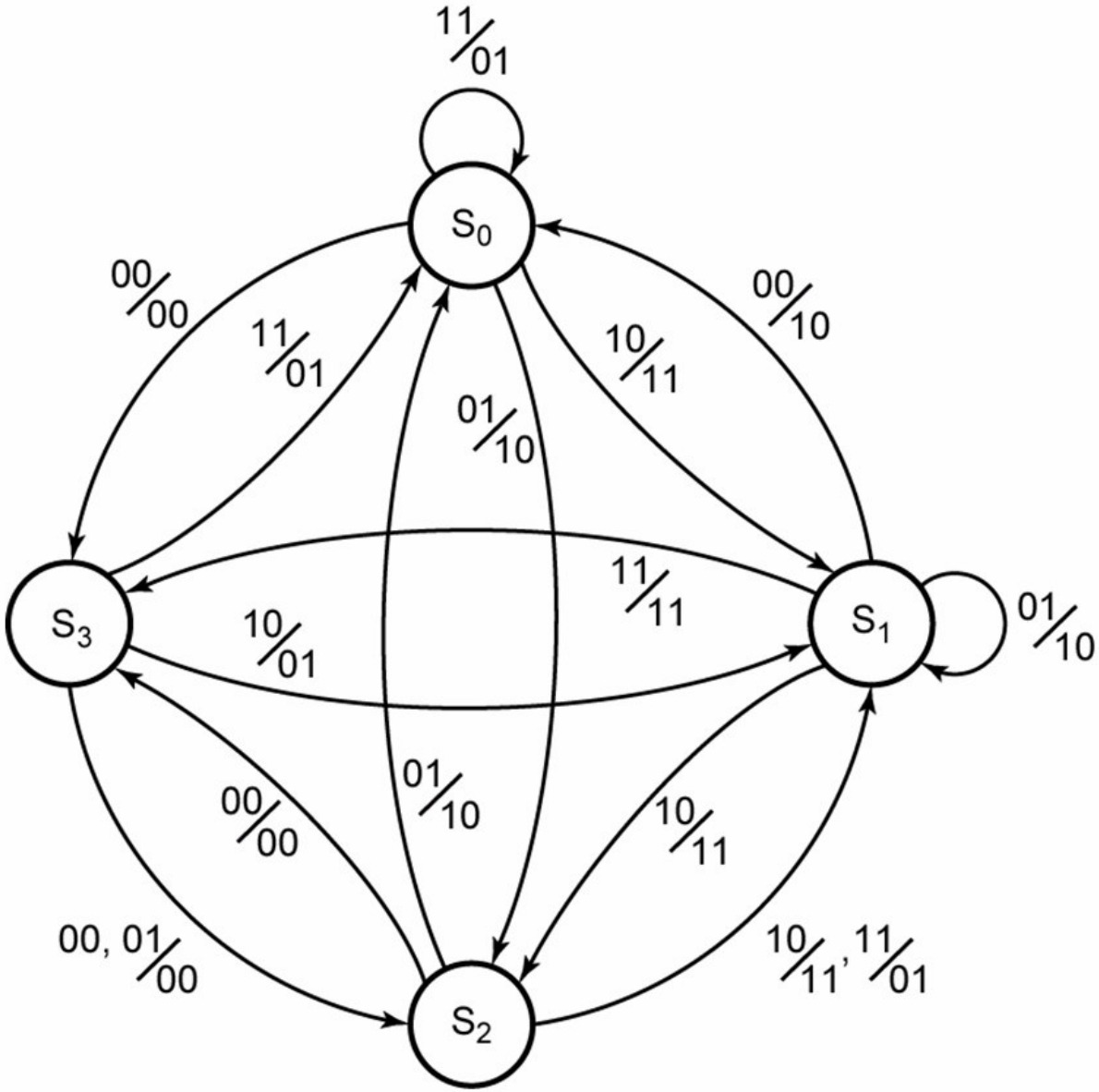


Figure 13-15: **State Graph for Table 13-4**

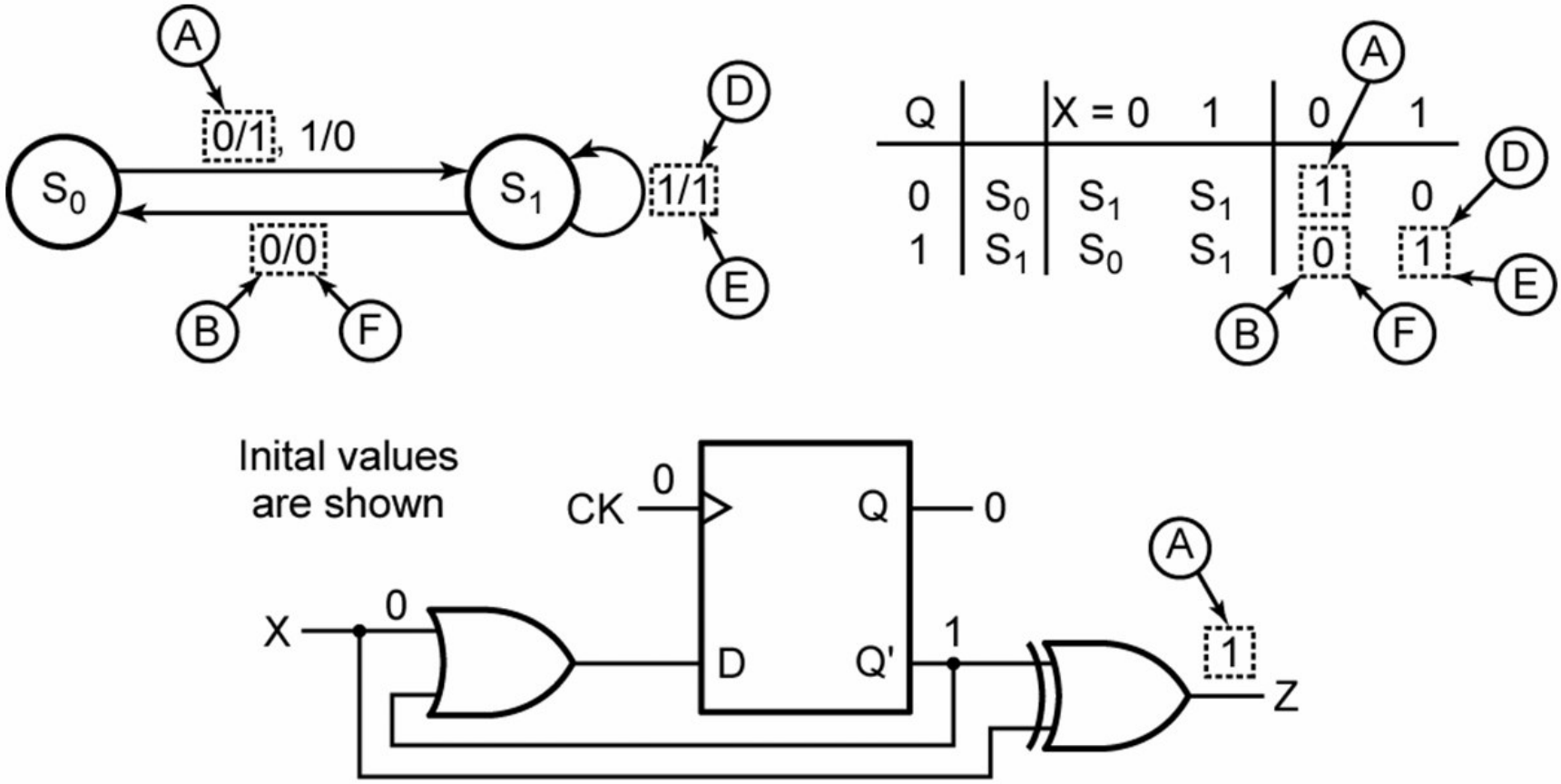


Figure 13-16

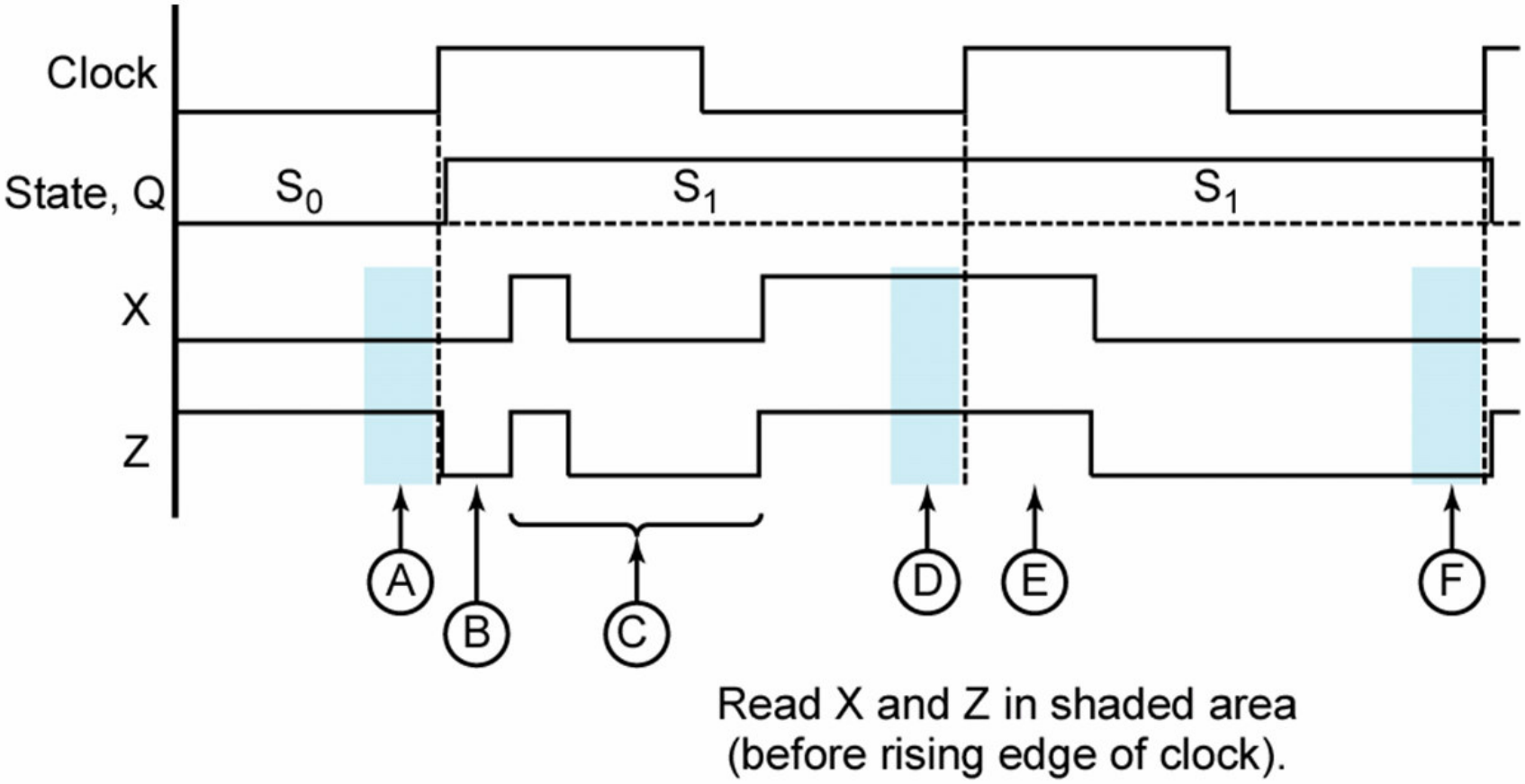


Figure 13-16

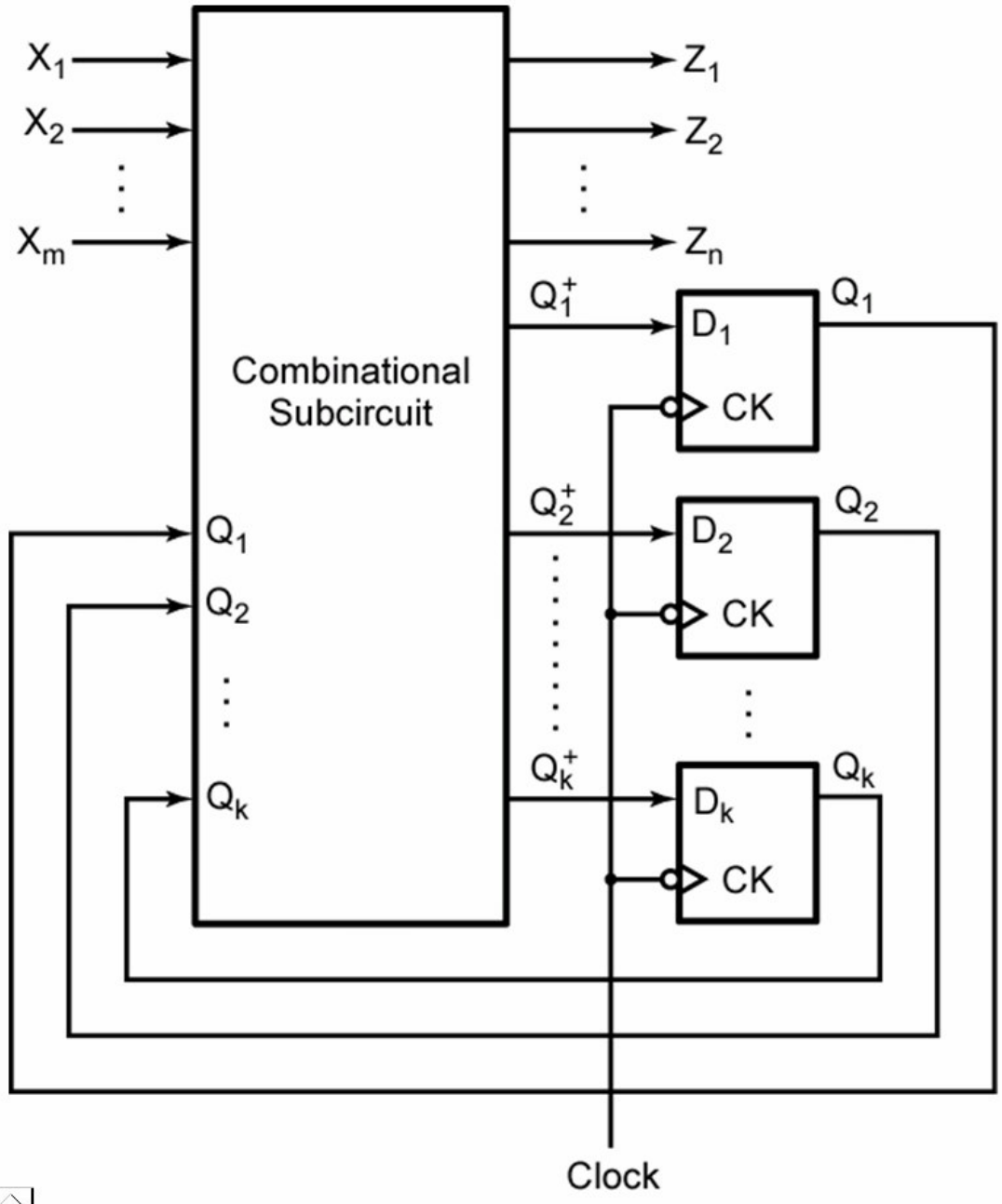


Figure 13-17:

General Model for Mealy Circuit Using Clocked D Flip-Flops

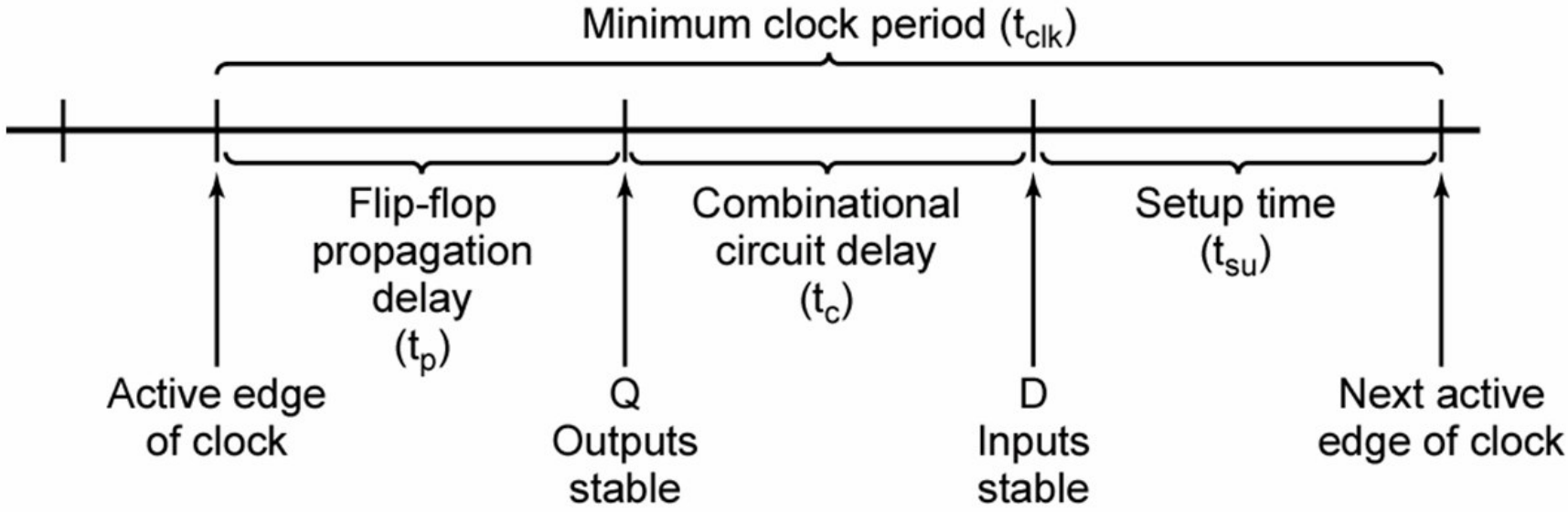


Figure 13-18: **Minimum Clock Period for a Sequential Circuit**

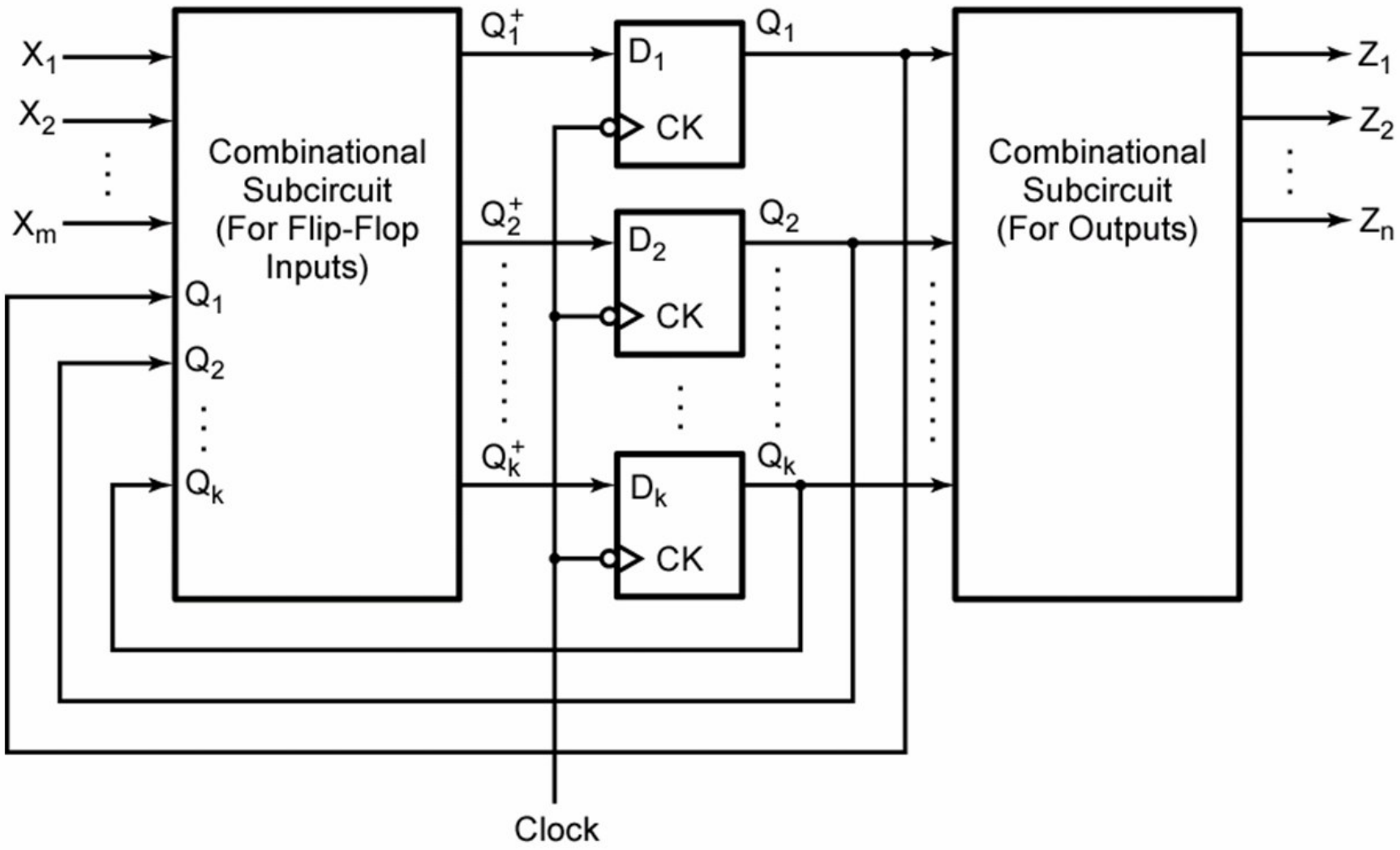


Figure 13-19: **General Model for Moore Circuit Using Clocked D Flip-Flops**

Table 13-5. State Table with Multiple Inputs and Outputs

Present State	Next State				Present Output (Z)			
	$X = 0$	1	2	3	$X = 0$	1	2	3
S_0	S_3	S_2	S_1	S_0	0	2	3	1
S_1	S_0	S_1	S_2	S_3	2	2	3	3
S_2	S_3	S_0	S_1	S_1	0	2	3	1
S_3	S_2	S_2	S_1	S_0	0	0	1	1