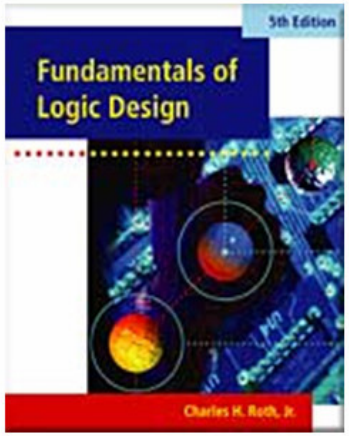
FIGURES FOR

CHAPTER 12

REGISTERS AND COUNTERS



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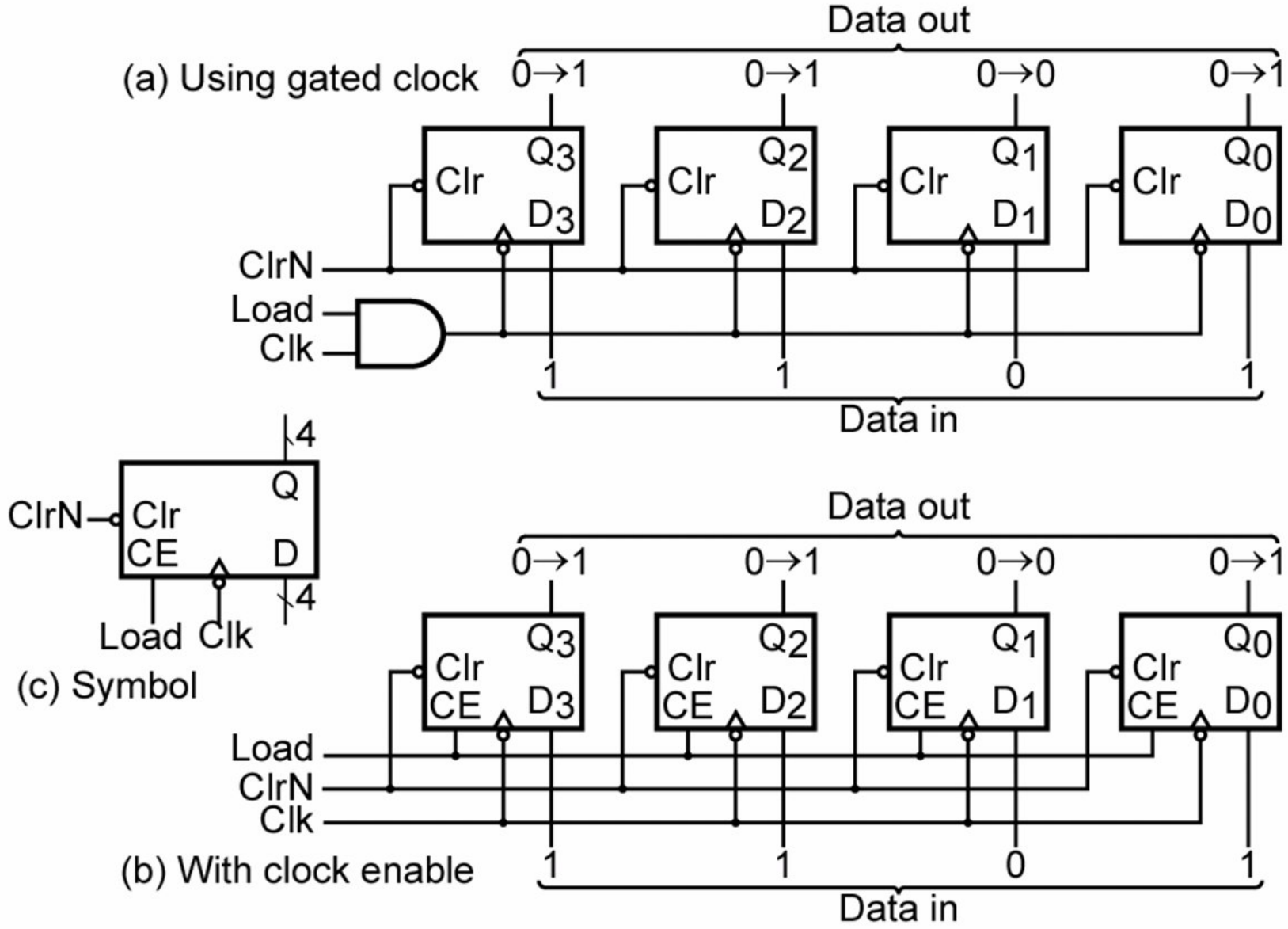


Figure 12-1: **4-Bit D Flip-Flop Registers with Data, Load, Clear, and Clock Inputs**

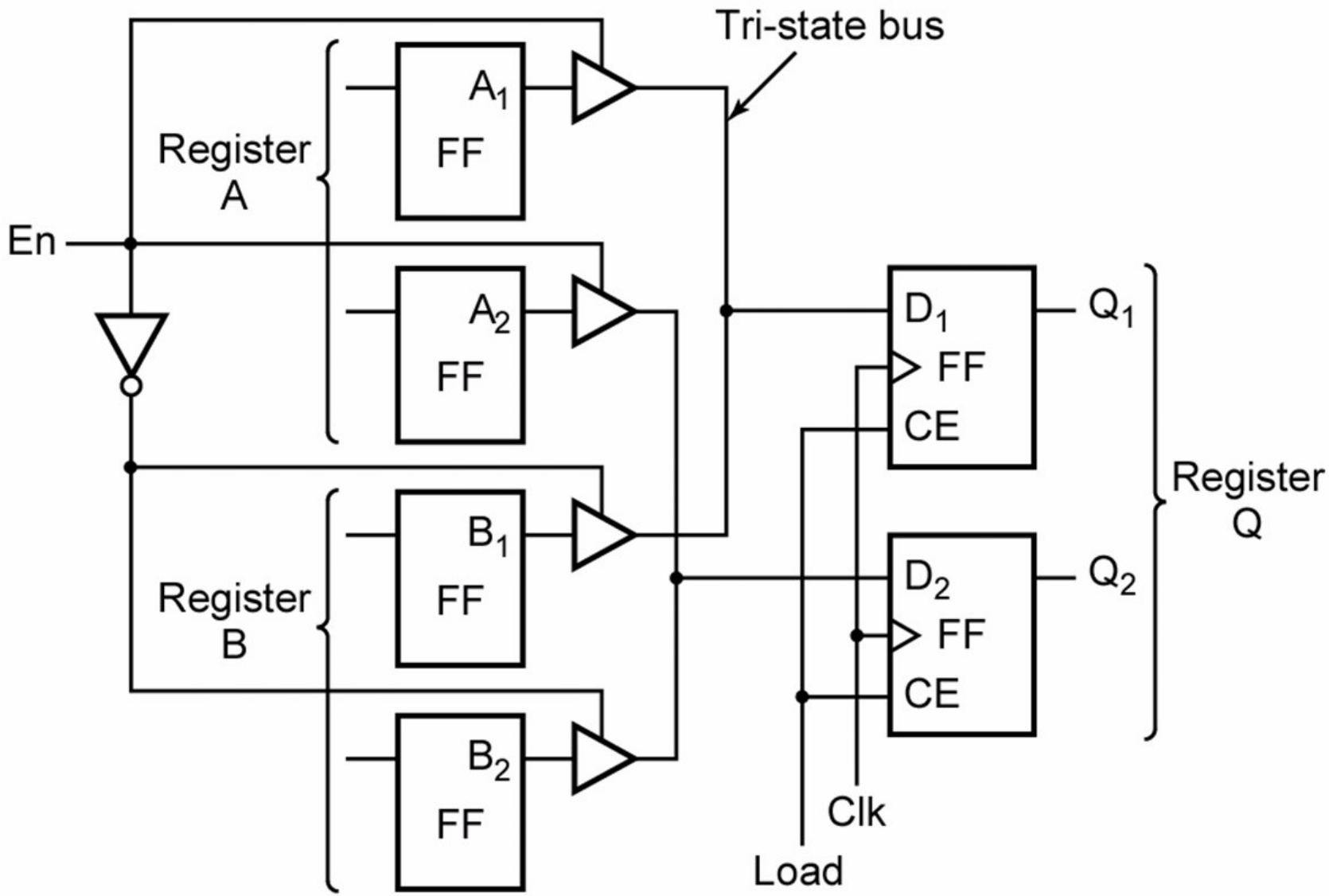


Figure 12-2: **Data Transfer Between Registers**

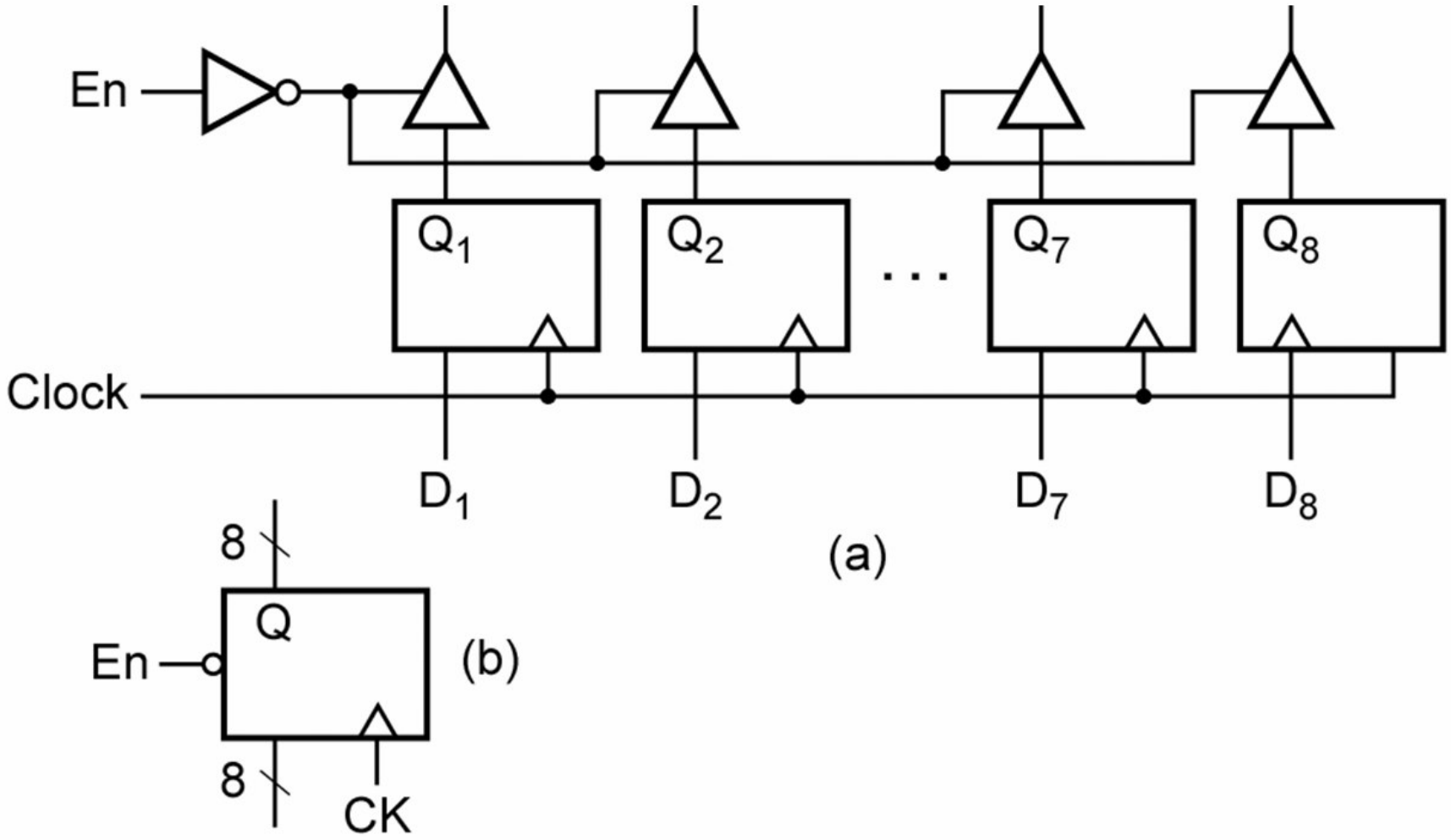


Figure 12-3: **Logic Diagram for 8-Bit Register with Tri-State Output**

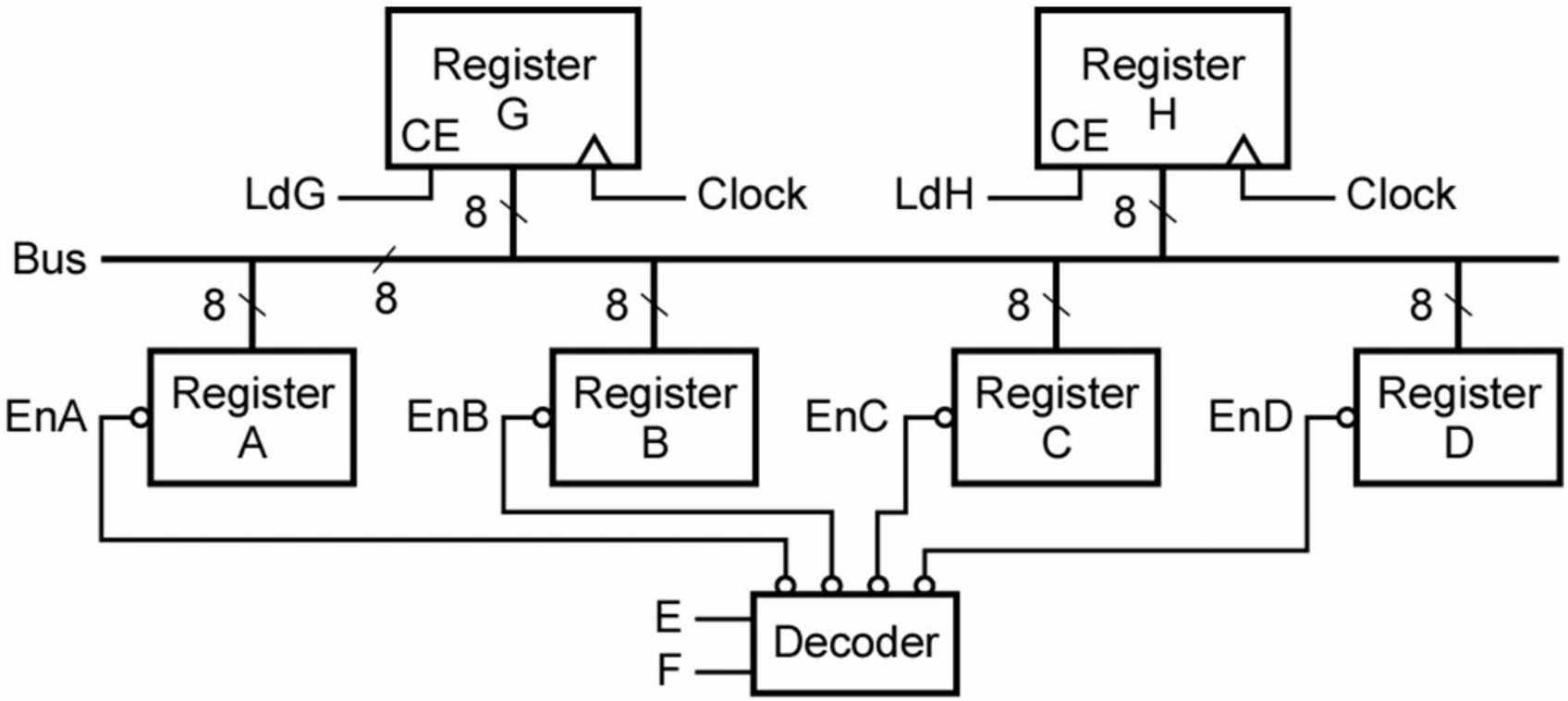


Figure 12-4: **Data Transfer Using a Tri-State Bus**

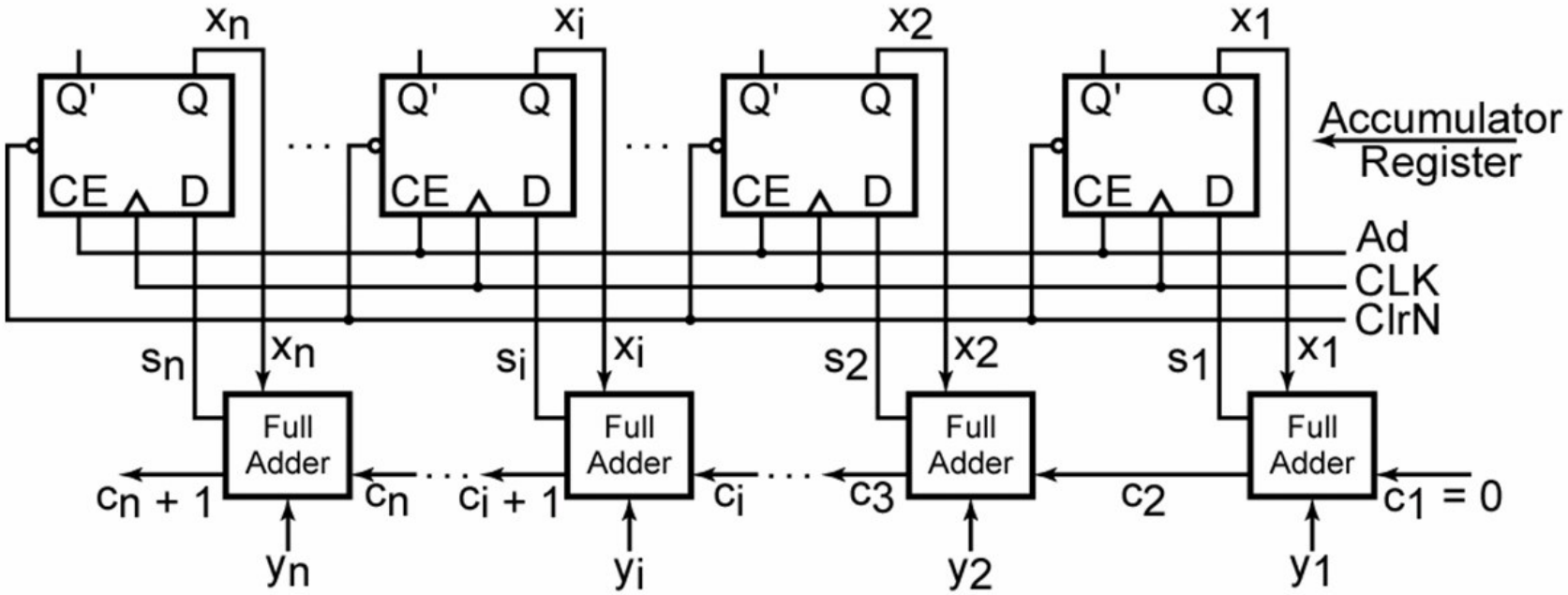


Figure 12-5: **N-Bit Parallel Adder with Accumulator**

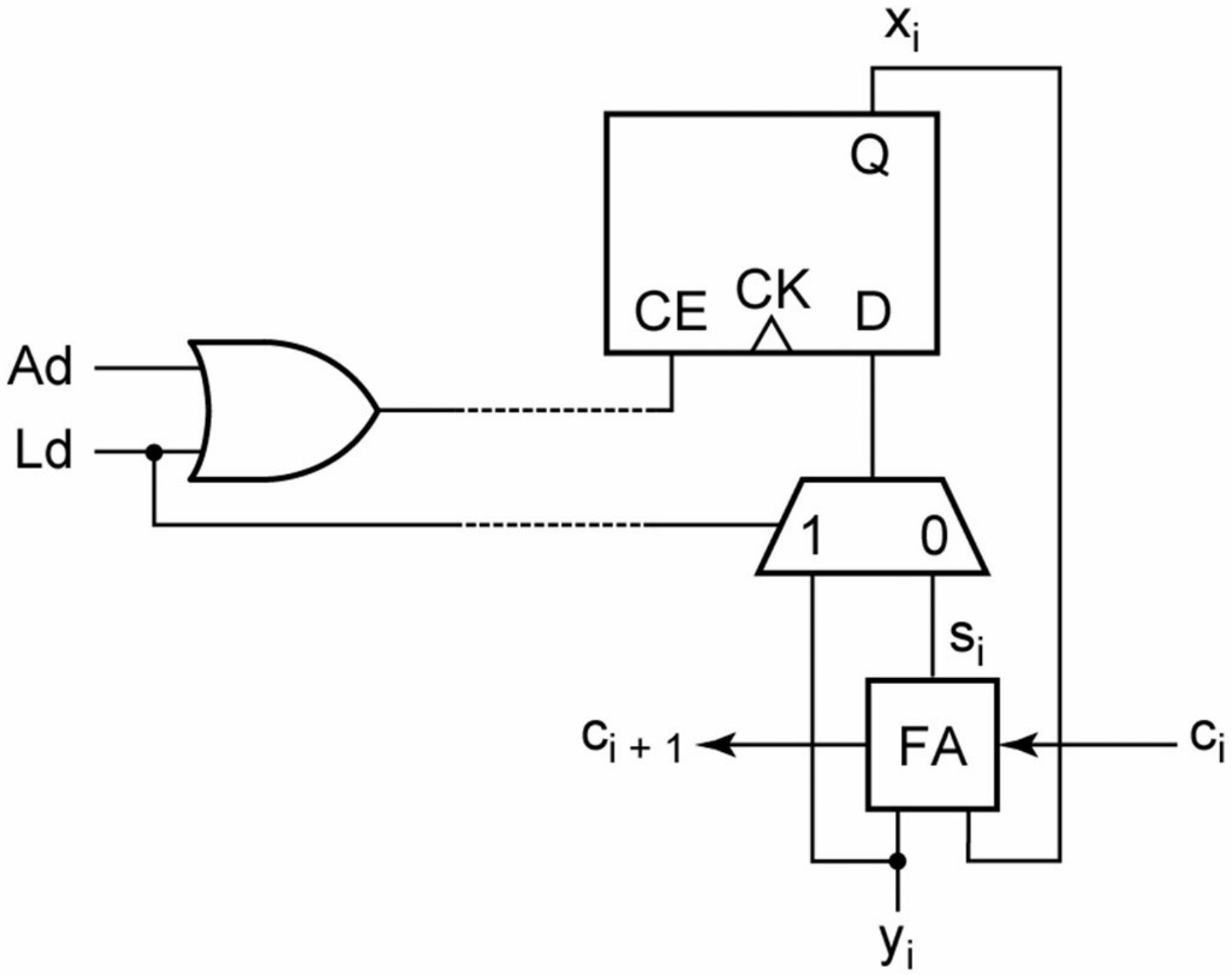
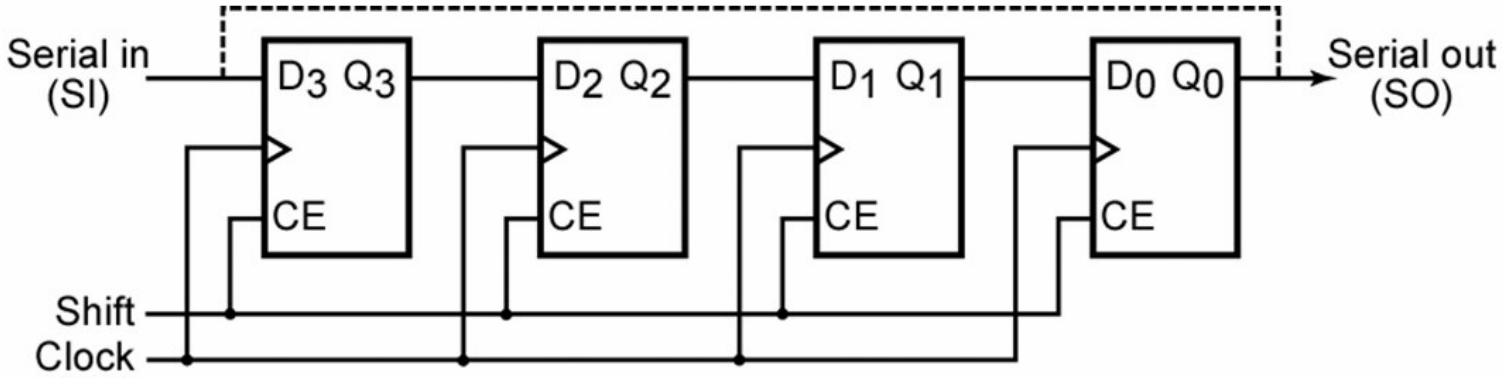
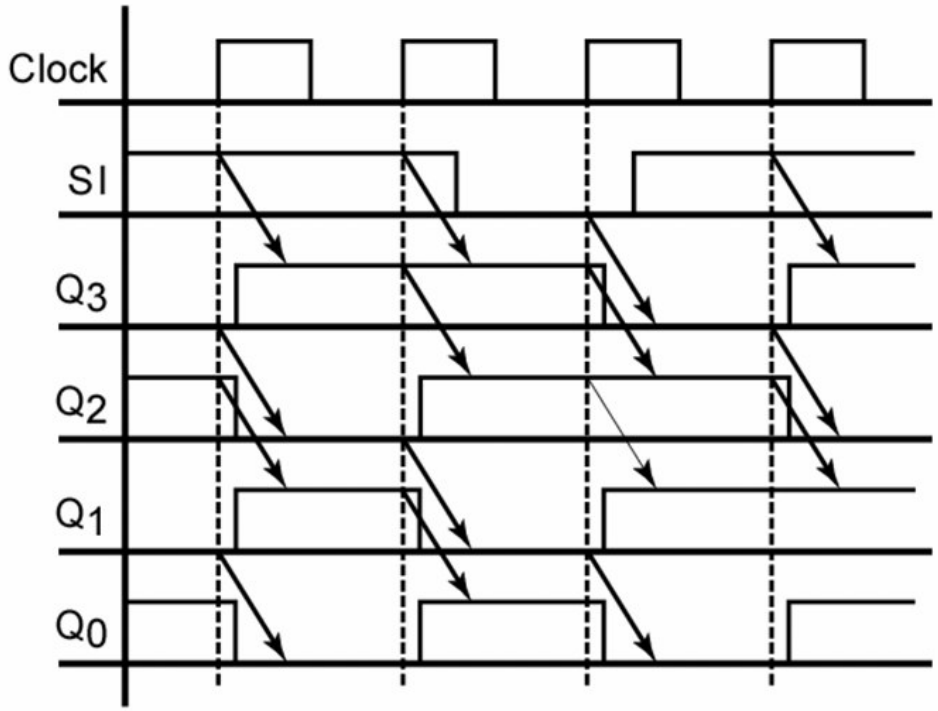


Figure 12-6: **Adder Cell with Multiplexer**



(a) Flip-flop connections



(b) Timing diagram

Figure 12-7: **Right-Shift Register**

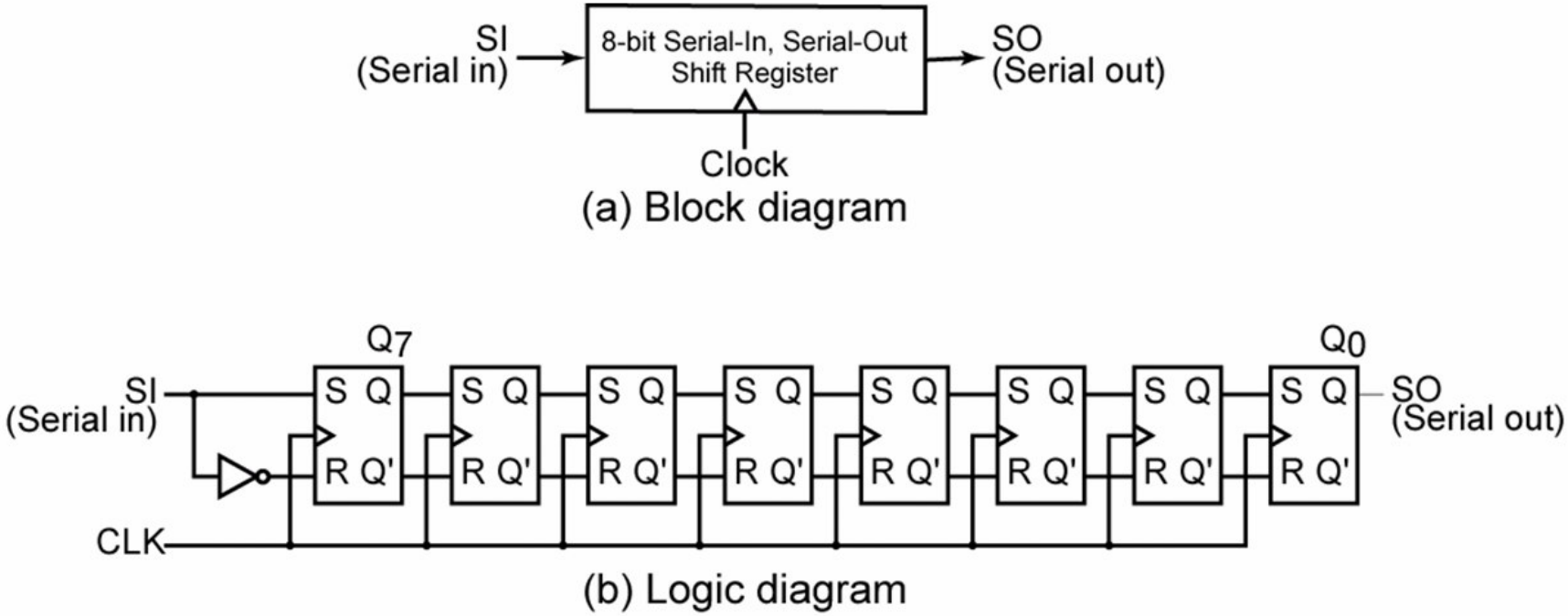


Figure 12-8: **8-Bit Serial-In, Serial-Out Shift Register**

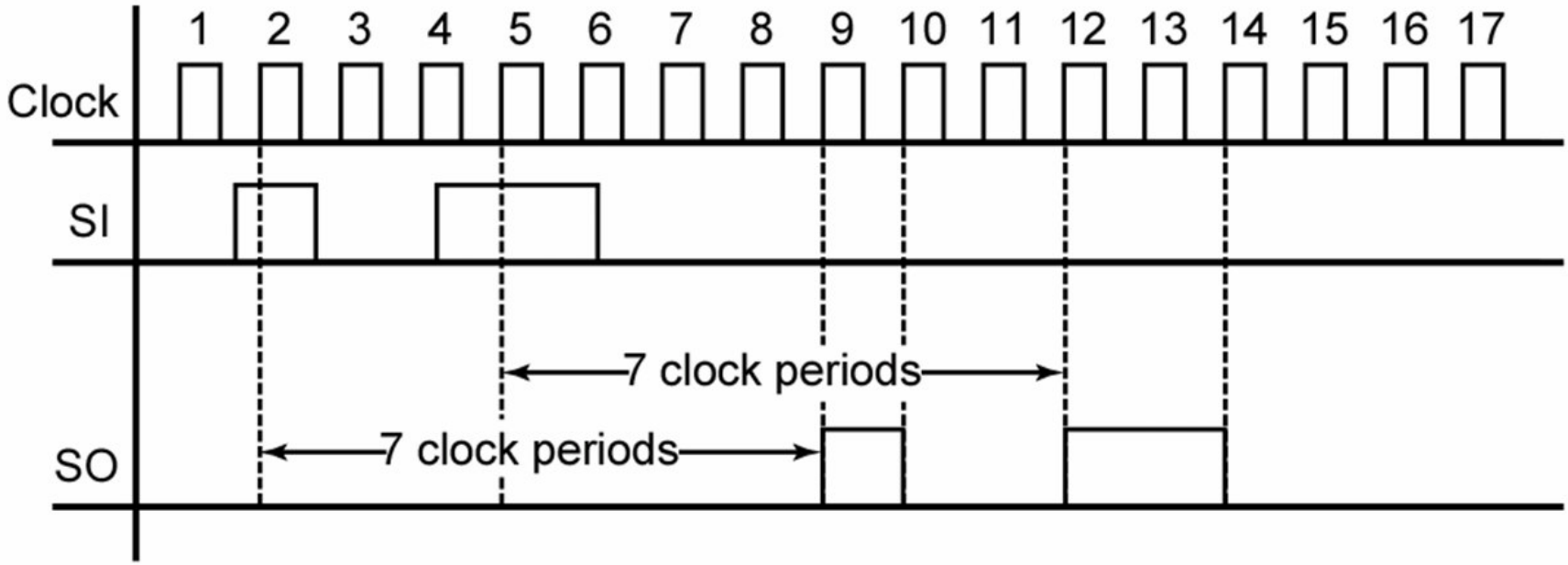


Figure 12-9: **Typical Timing Diagram for Shift Register of Figure 12-8**

Figure 12-10: Parallel-In, Parallel-Out Right Shift Register

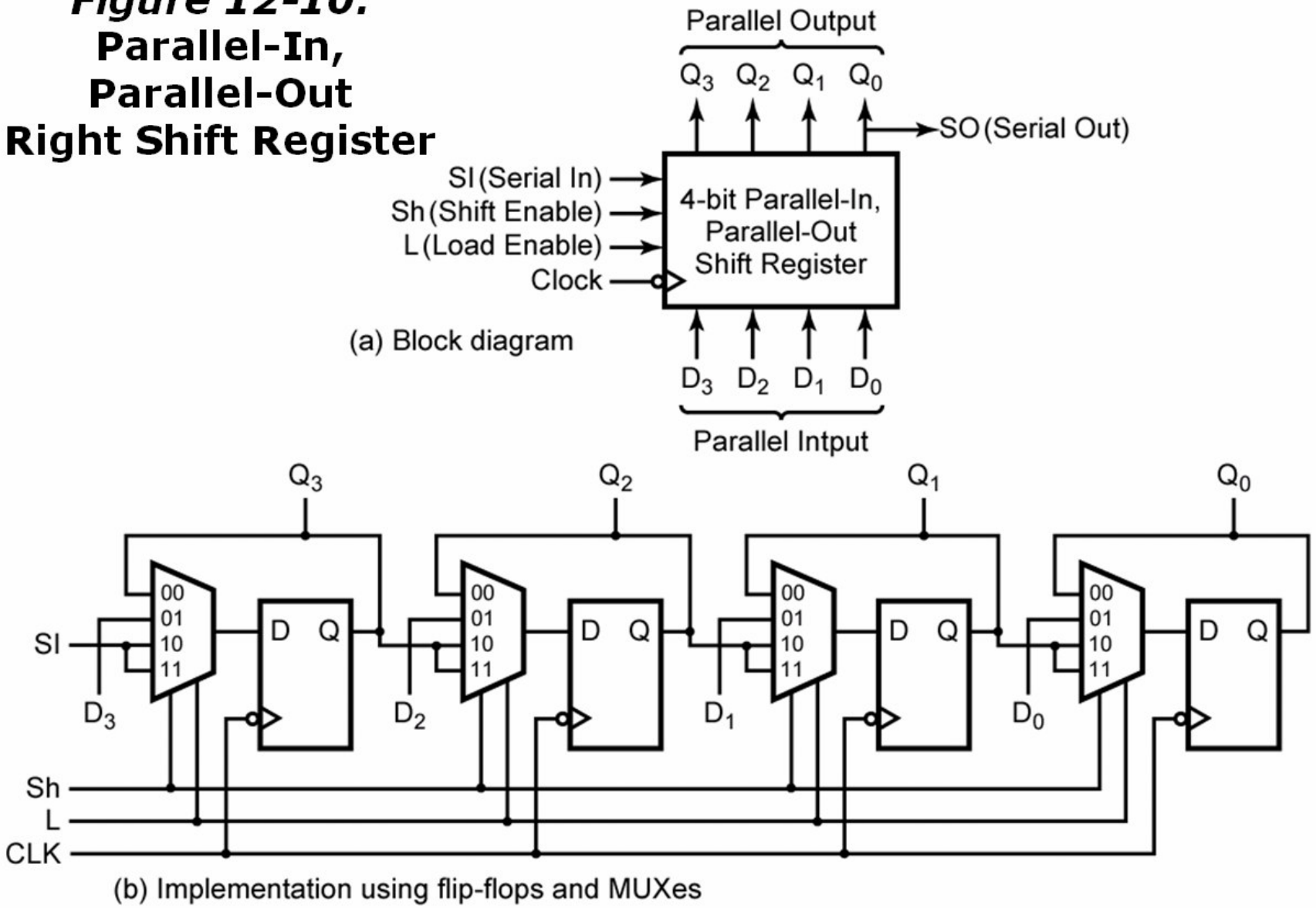


Table 12-1: Shift Register Operation

Inputs		Next State				Action
Sh (Shift)	Ld (Load)	Q_3^+	Q_2^+	Q_1^+	Q_0^+	
0	0	Q_3	Q_2	Q_1	Q_0	no change
0	1	D_3	D_2	D_1	D_0	load
1	X	SI	Q_3	Q_2	Q_1	right shift

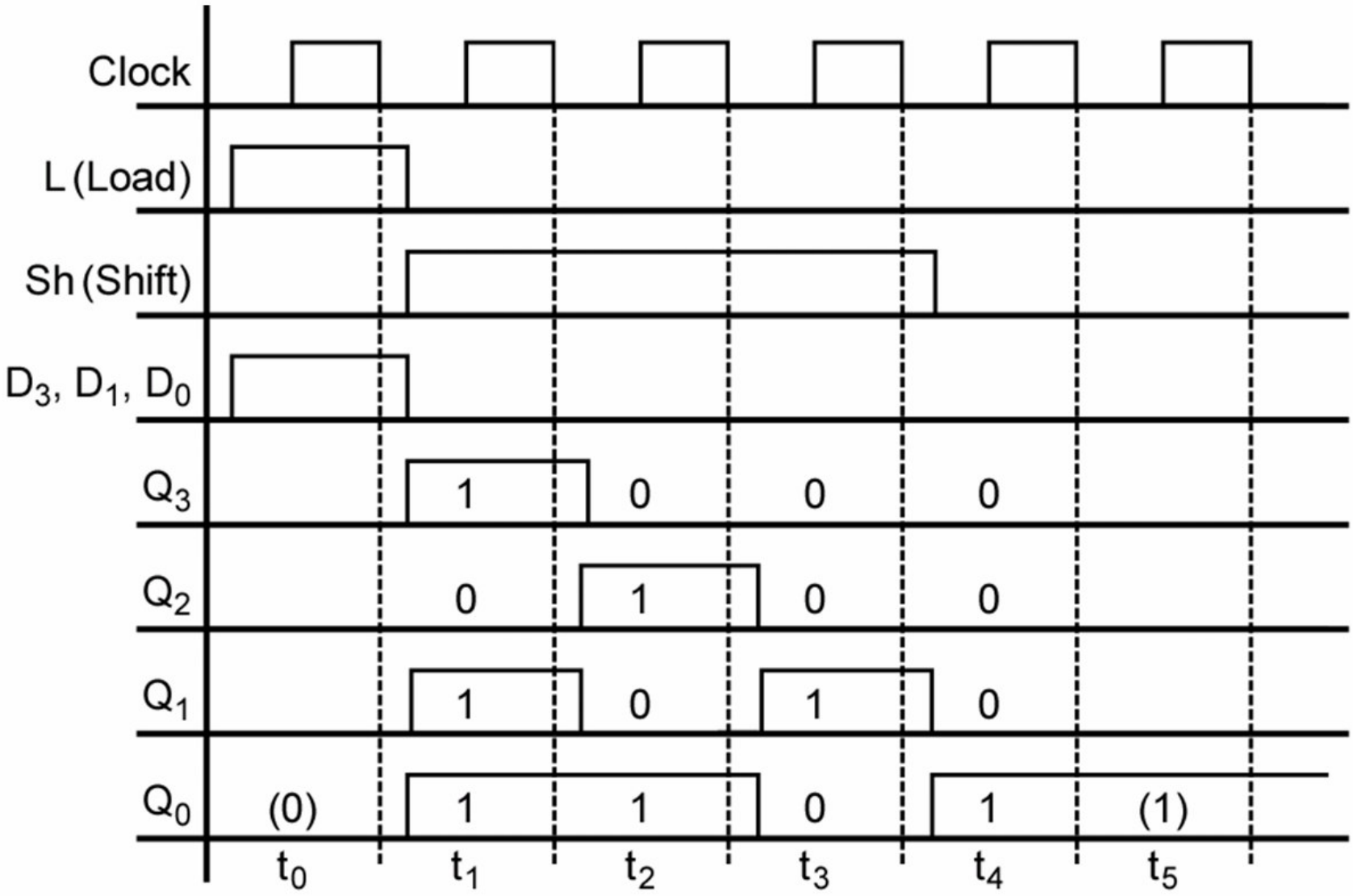
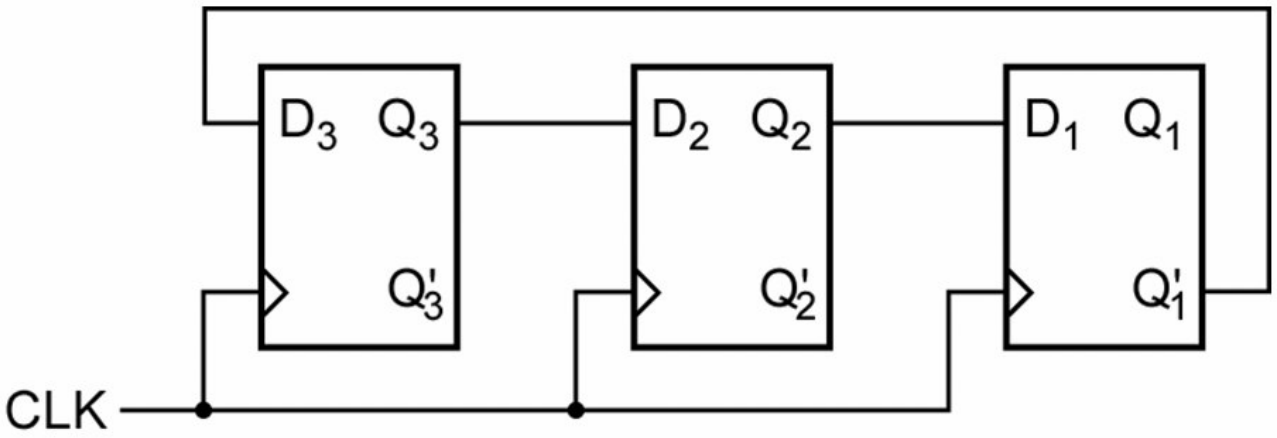
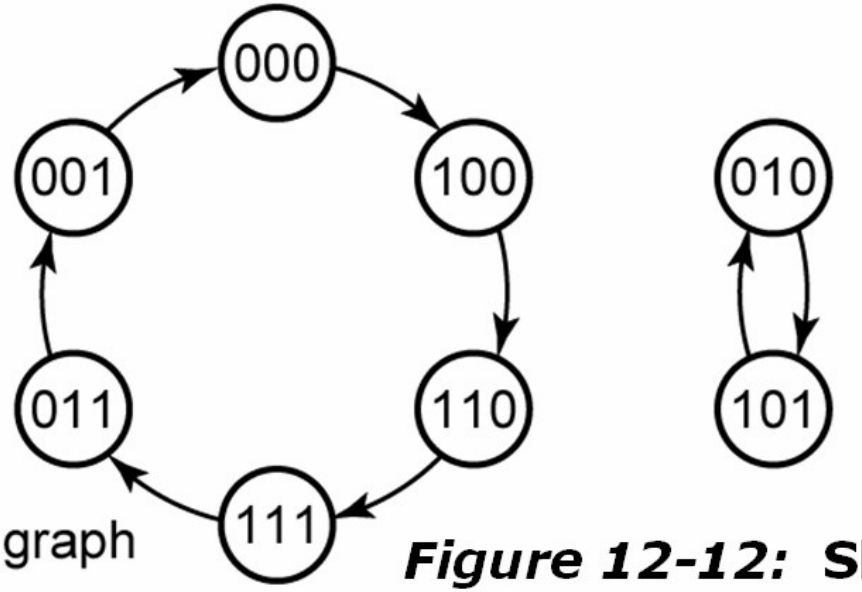


Figure 12-11: **Timing Diagram for Shift Register**



(a) Flip-flop connections



(b) State graph

Figure 12-12: **Shift Register with Inverted Feedback**

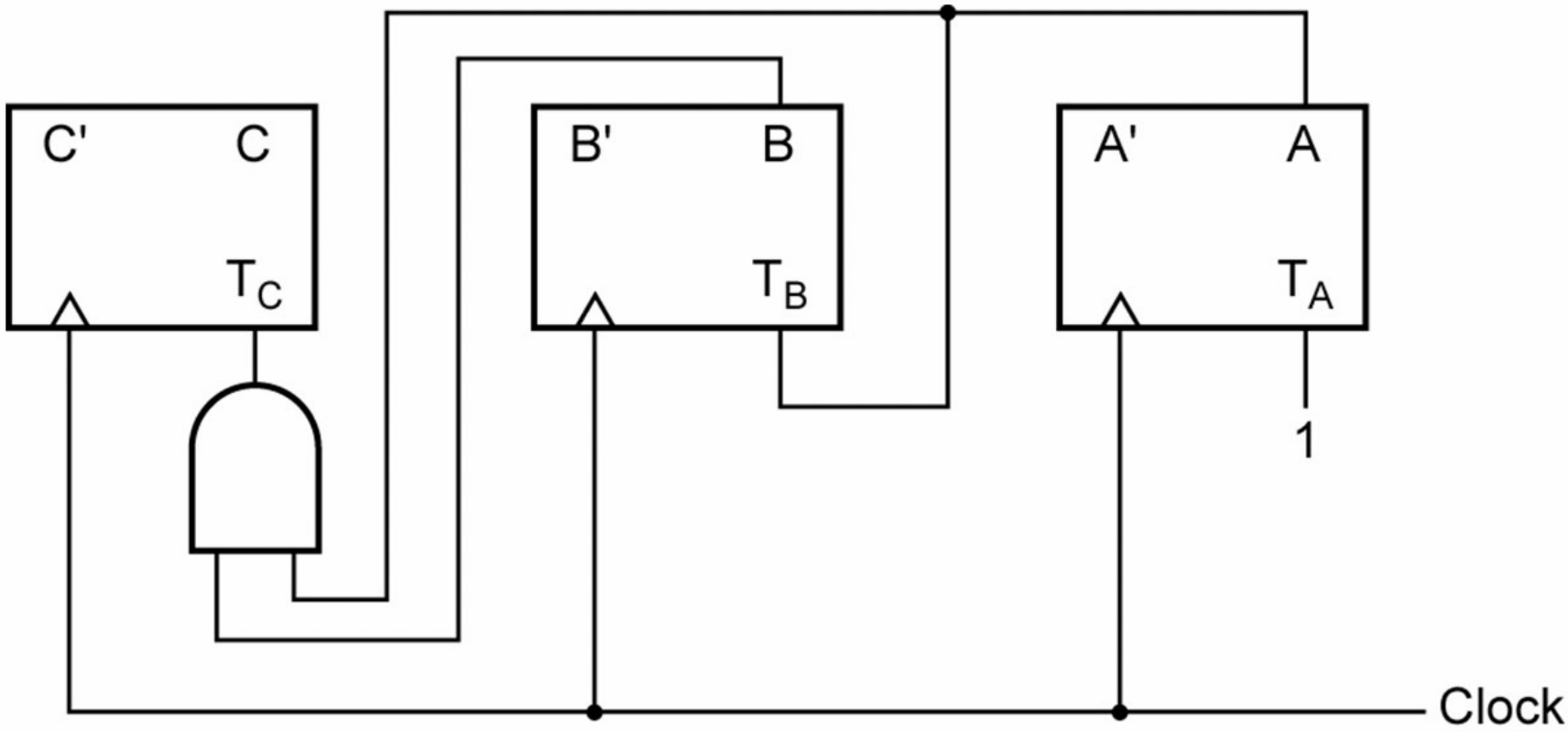
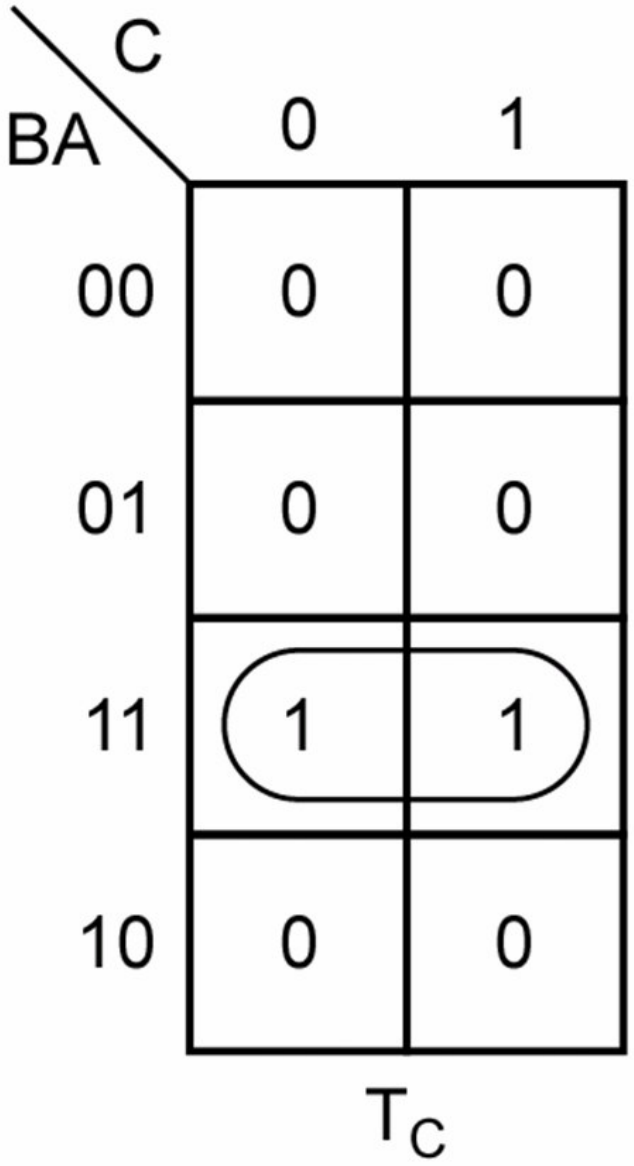


Figure 12-13: **Synchronous Binary Counter**

Table 12-2 State Table for Binary Counter

Present State			Next State			Flip-Flop Inputs		
C	B	A	C^+	B^+	A^+	T_C	T_B	T_A
0	0	0	0	0	1	0	0	1
0	0	1	0	1	0	0	1	1
0	1	0	0	1	1	0	0	1
0	1	1	1	0	0	1	1	1
1	0	0	1	0	1	0	0	1
1	0	1	1	1	0	0	1	1
1	1	0	1	1	1	0	0	1
1	1	1	0	0	0	1	1	1



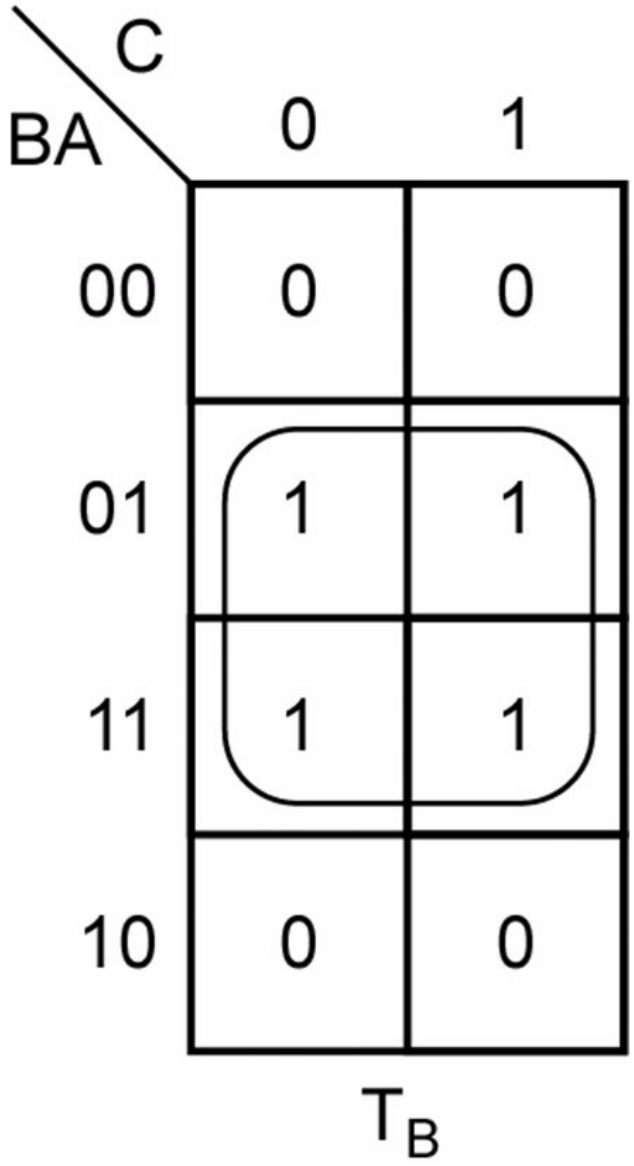


Figure 12-14: **Karnaugh Maps for Binary Counter**

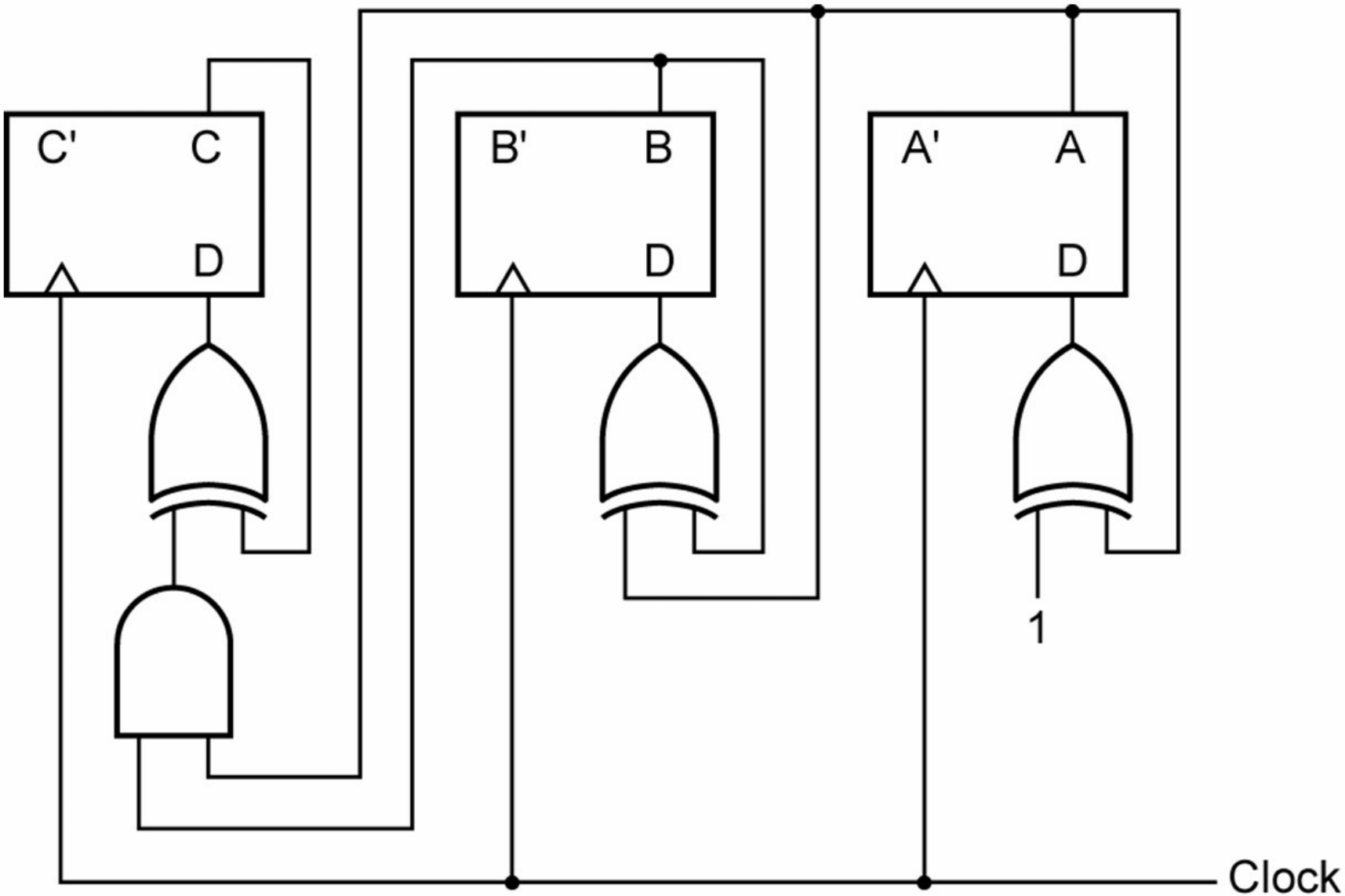


Figure 12-15: **Binary Counter with D Flip-Flops**

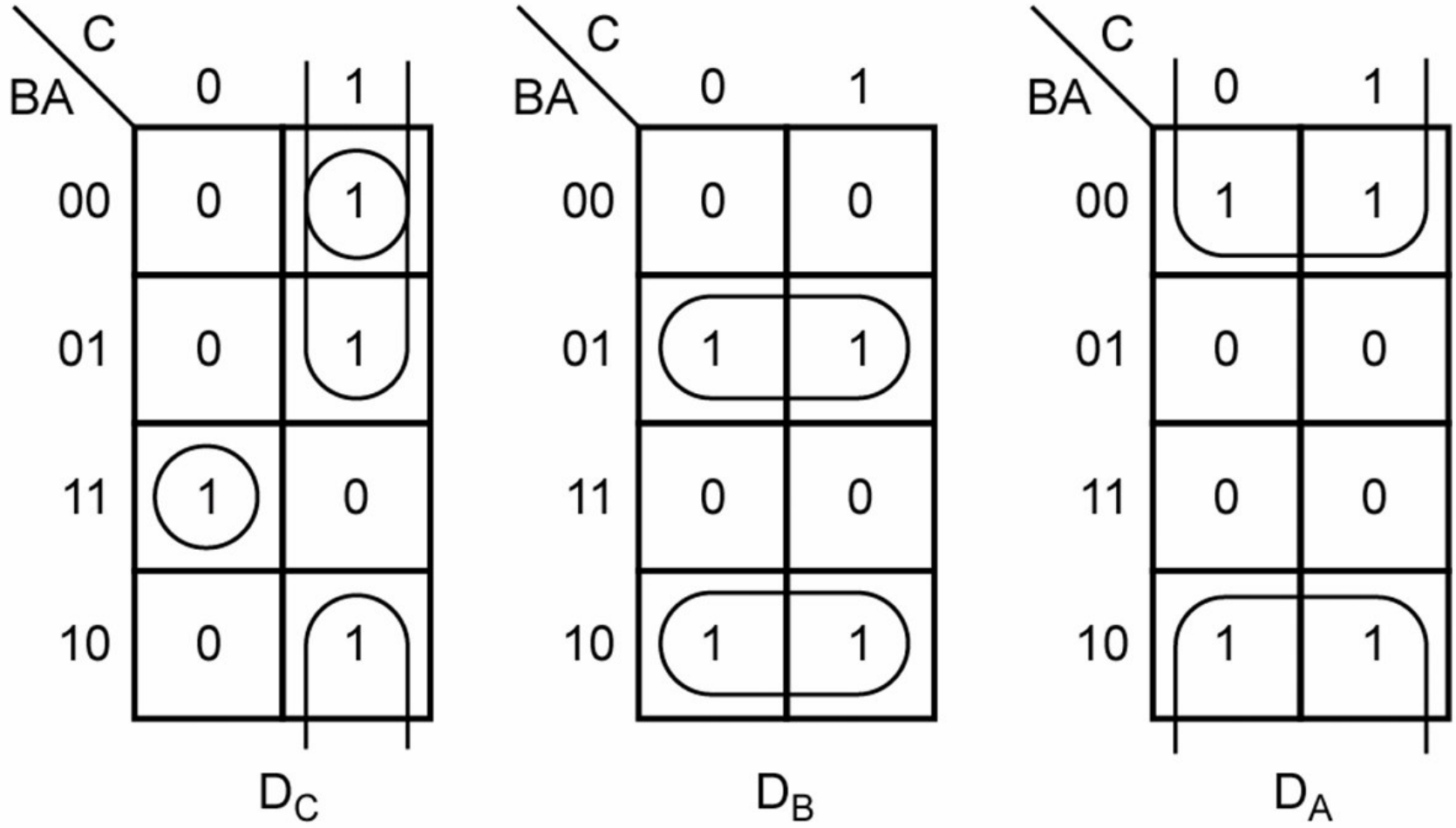
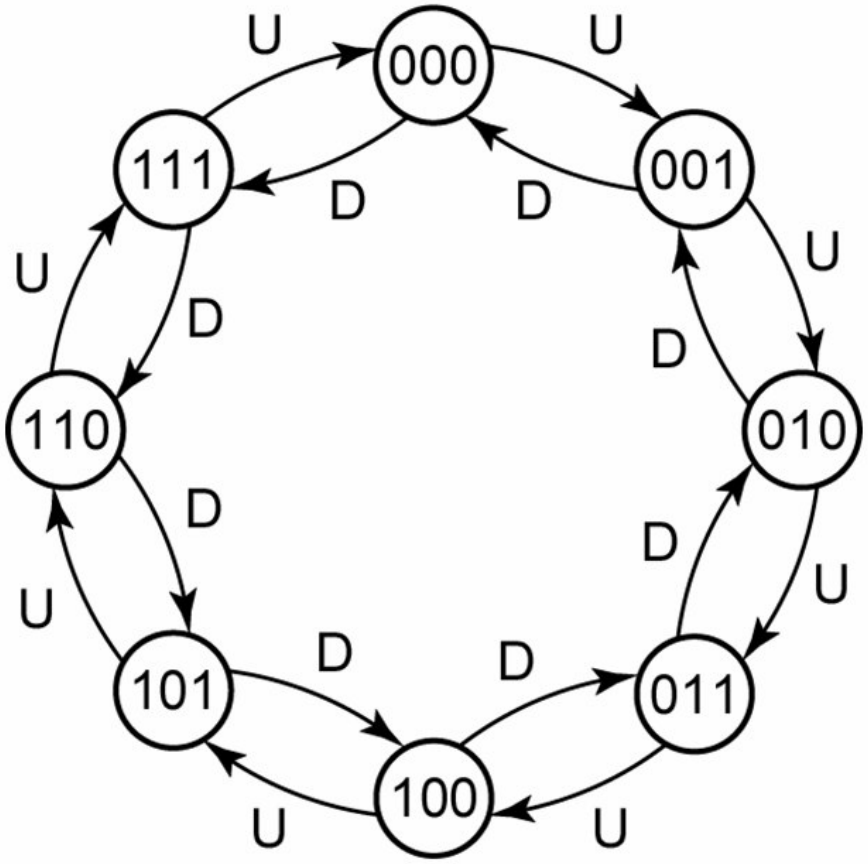


Figure 12-16: **Karnaugh Maps for D Flip-Flops**



CBA	$C^+B^+A^+$	
	U	D
000	001	111
001	010	000
010	011	001
011	100	010
100	101	011
101	110	100
110	111	101
111	000	110

Figure 12-17: **State Graph and Table for Up-Down Counter**

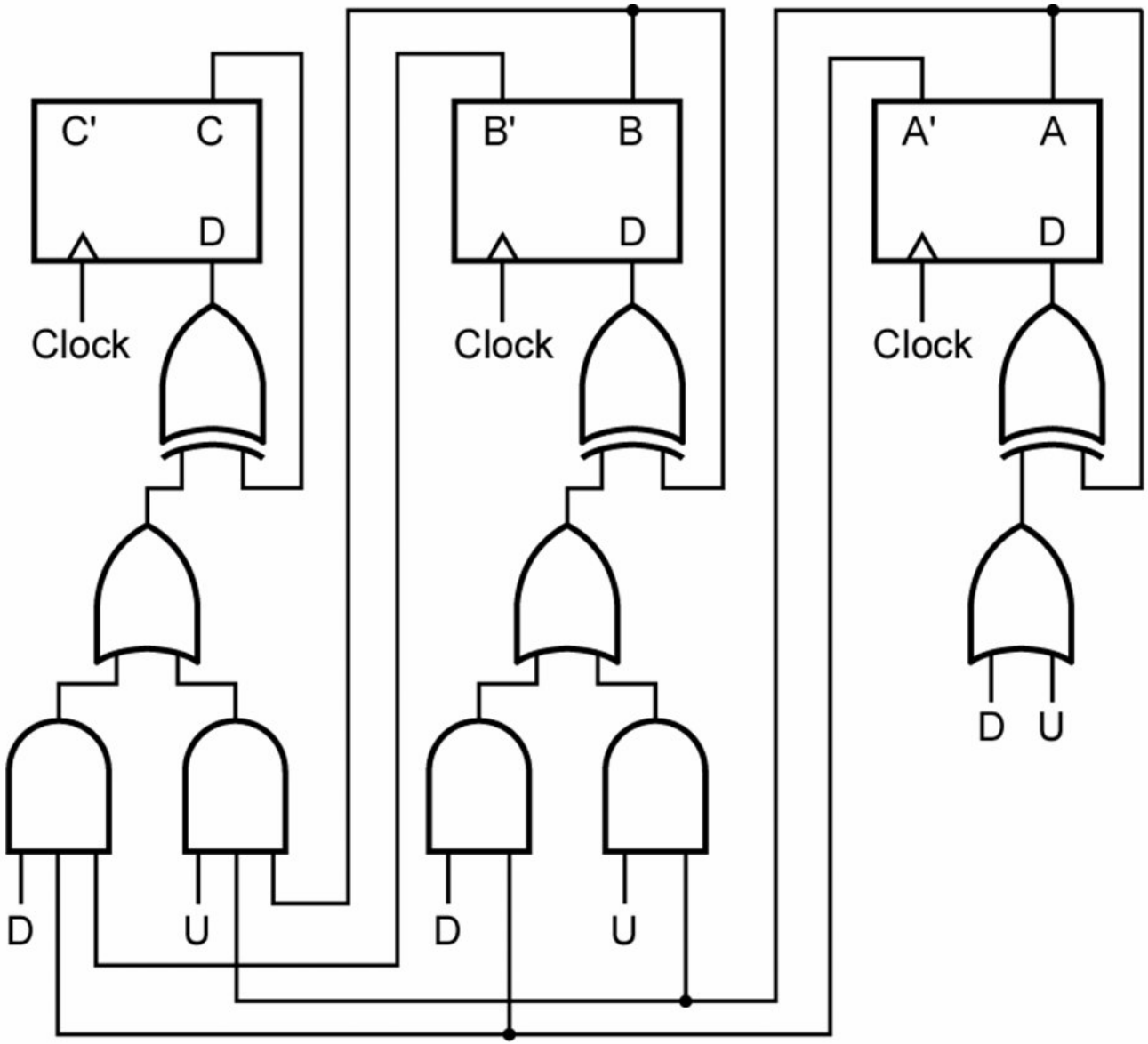
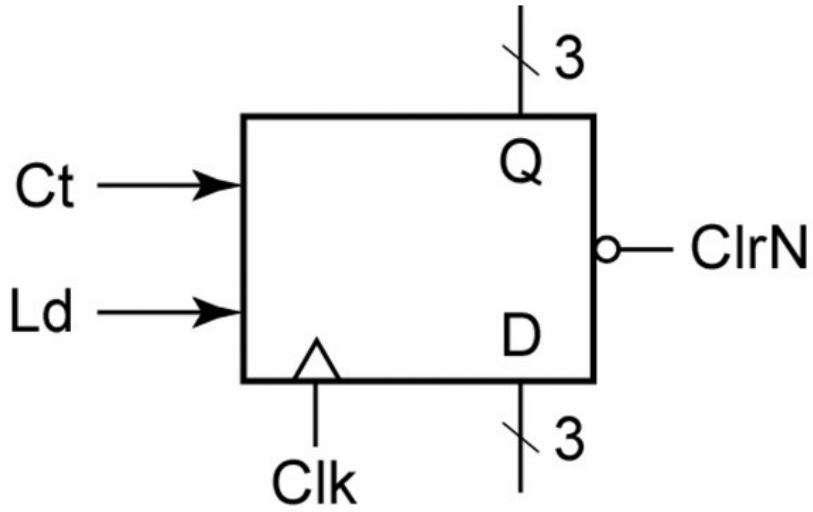


Figure 12-18: **Binary Up-Down Counter**



(a)

ClrN	Ld	Ct	C^+	B^+	A^+	
0	X	X	0	0	0	
1	1	X	D_C	D_B	D_A	(load)
1	0	0	C	B	A	(no change)
1	0	1	Present state + 1			

(b)

Figure 12-19ab: **Loadable Counter with Count Enable**

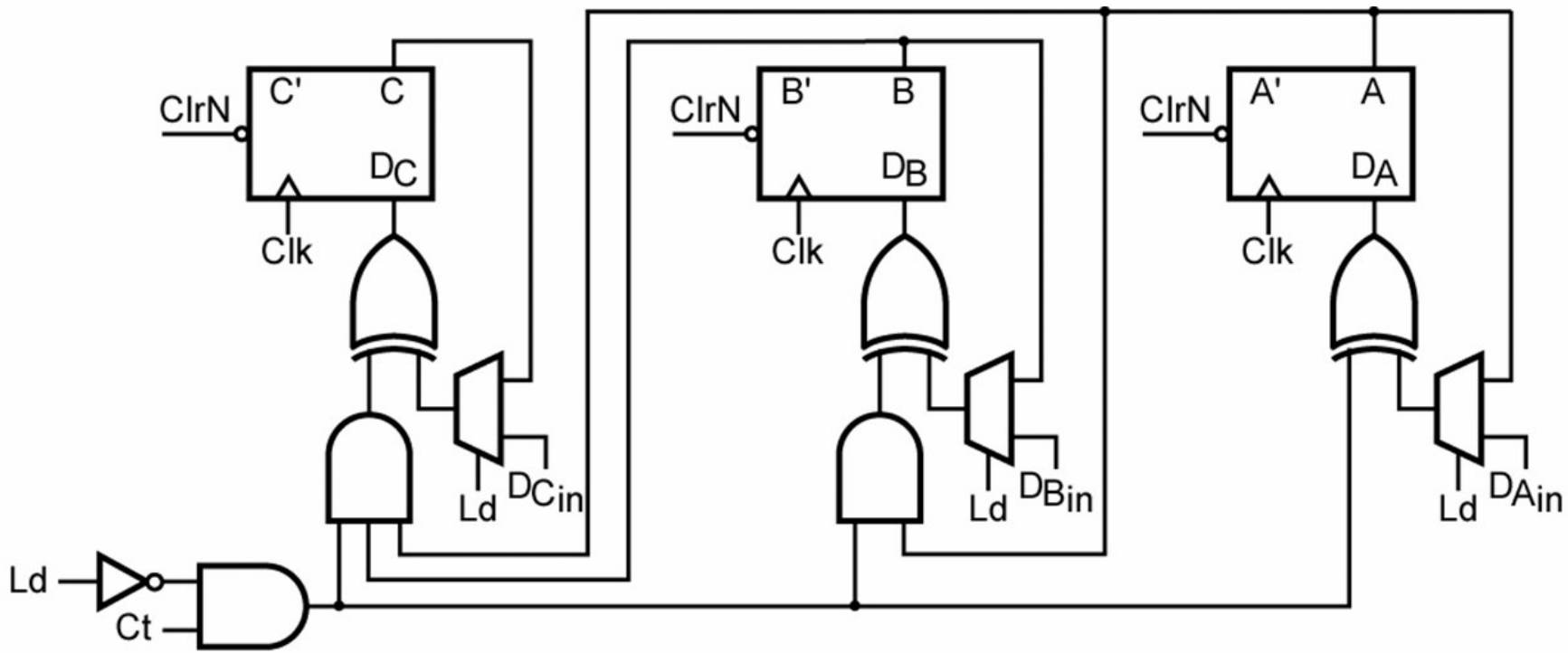


Figure 12-20: **Circuit for Figure 12-19**

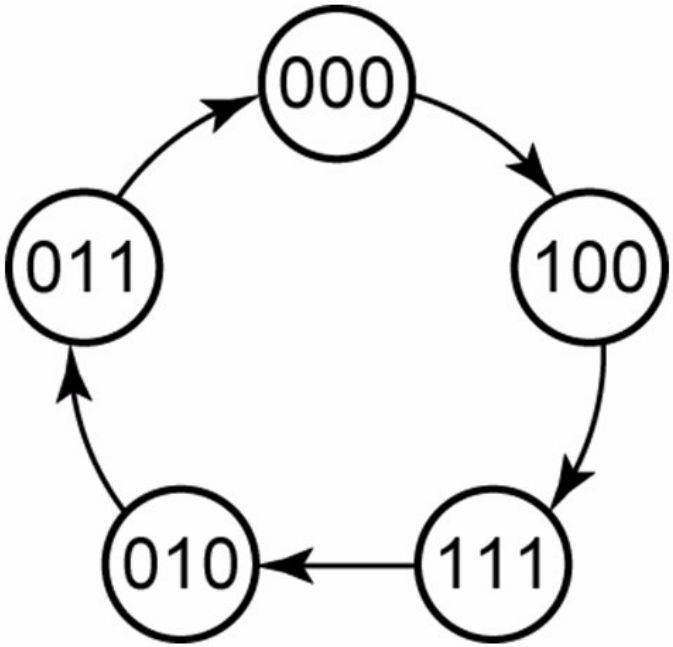


Figure 12-21:
State Graph for Counter

Table 12-3: State Table for Figure 12-21

C	B	A	C^+	B^+	A^+
0	0	0	1	0	0
0	0	1	-	-	-
0	1	0	0	1	1
0	1	1	0	0	0
1	0	0	1	1	1
1	0	1	-	-	-
1	1	0	-	-	-
1	1	1	0	1	0

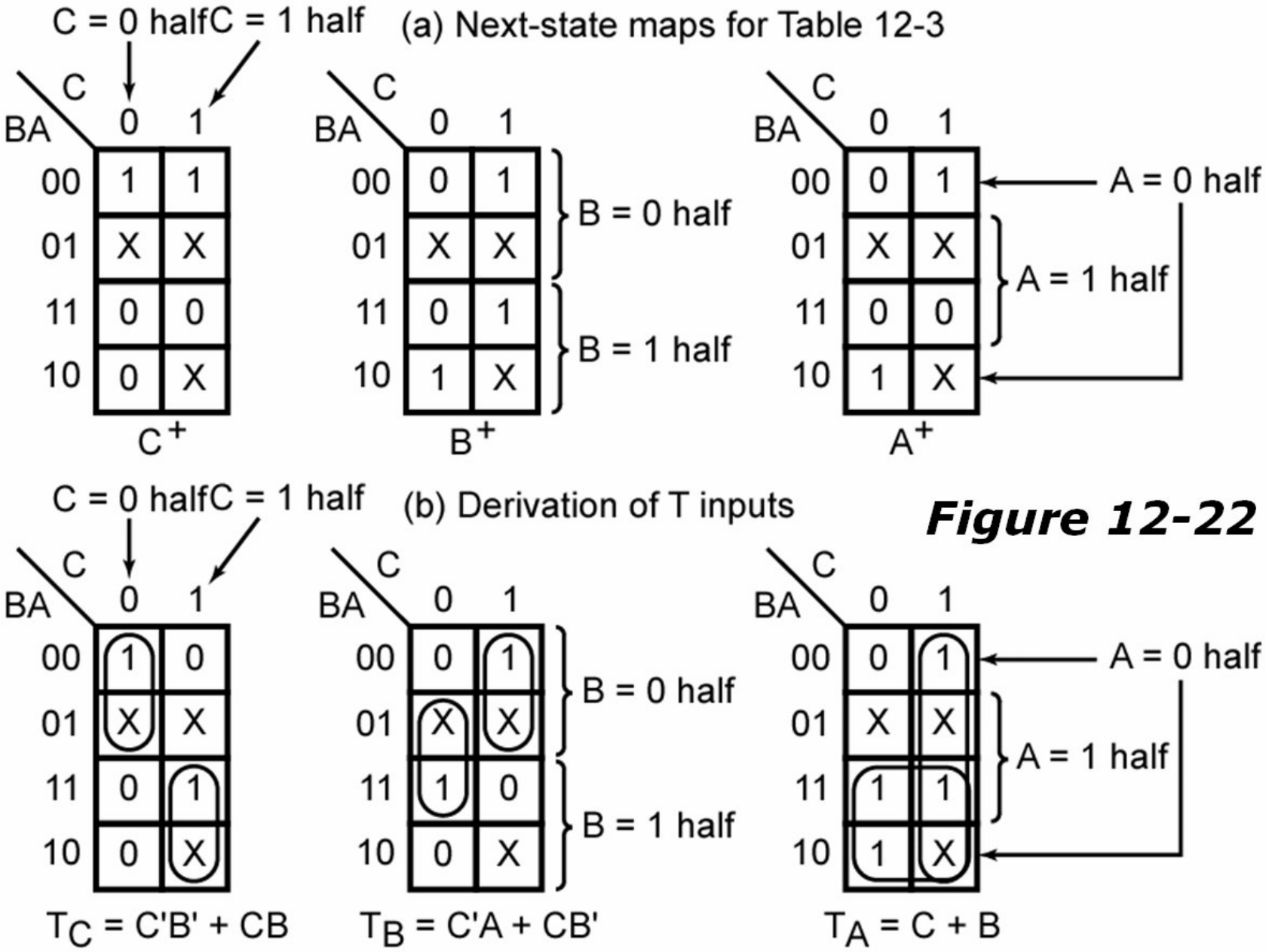


Figure 12-22

Table 12-4. Input for T Flip-Flop

Q	Q^+	T
0	0	0
0	1	1
1	0	1
1	1	0

$$T = Q^+ \oplus Q$$

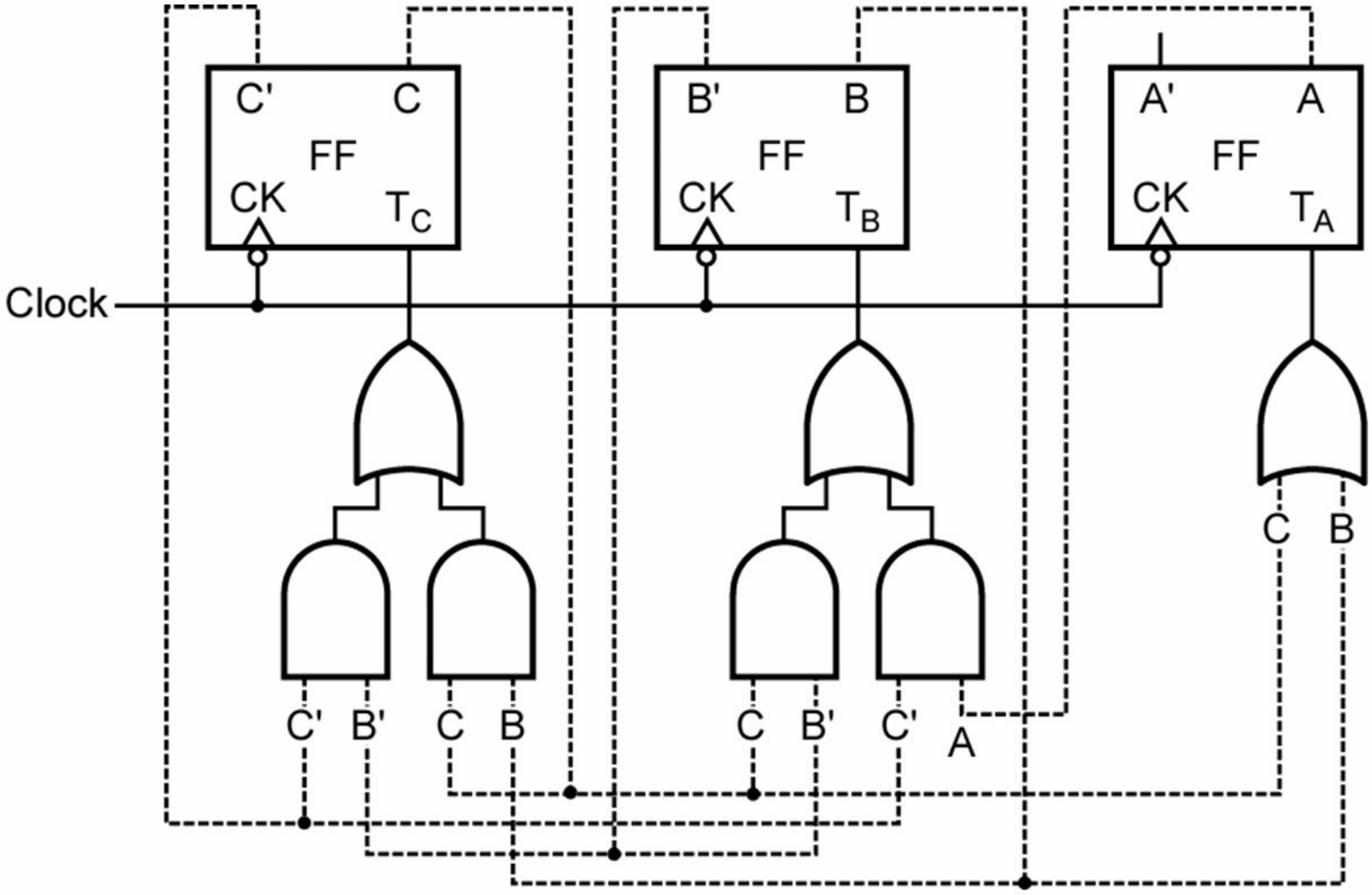


Figure 12-23: **Counter Using T Flip-Flops**

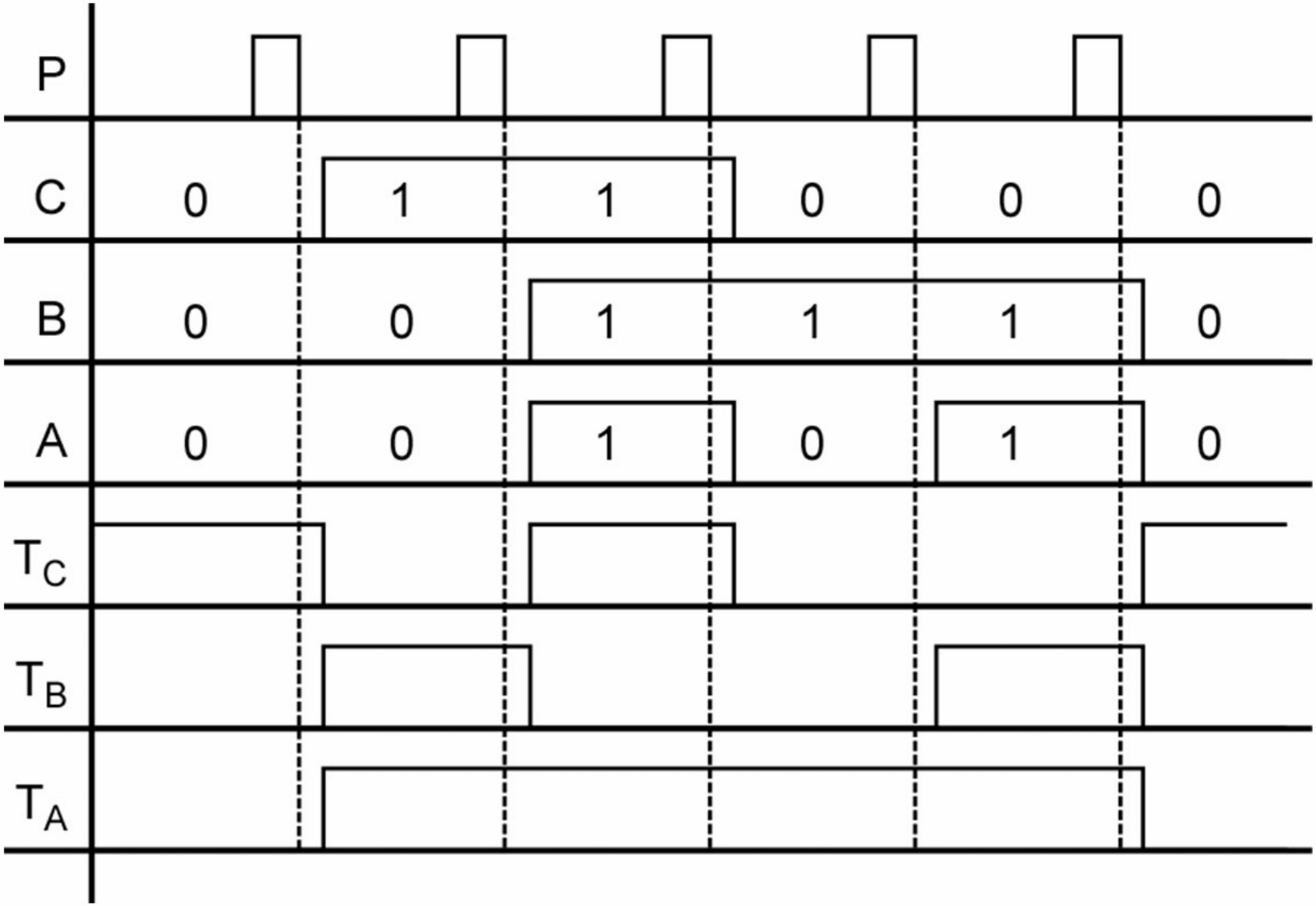


Figure 12-24: **Timing Diagram for Figure 12-23**

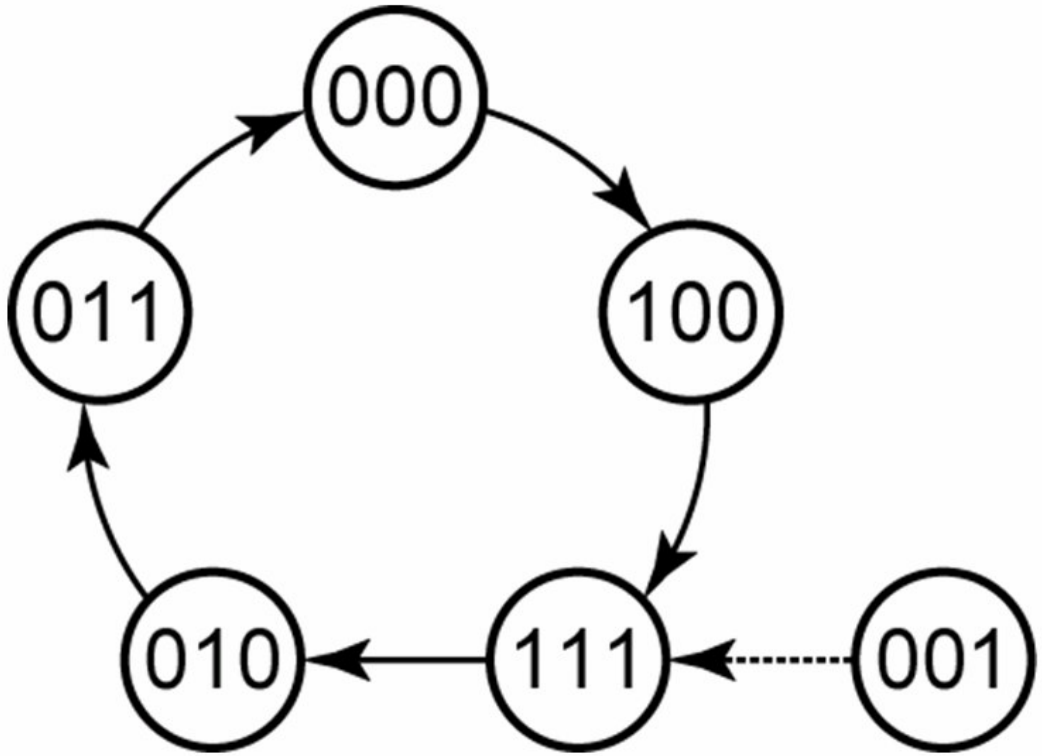


Figure 12-25: **State Graph for Counter**

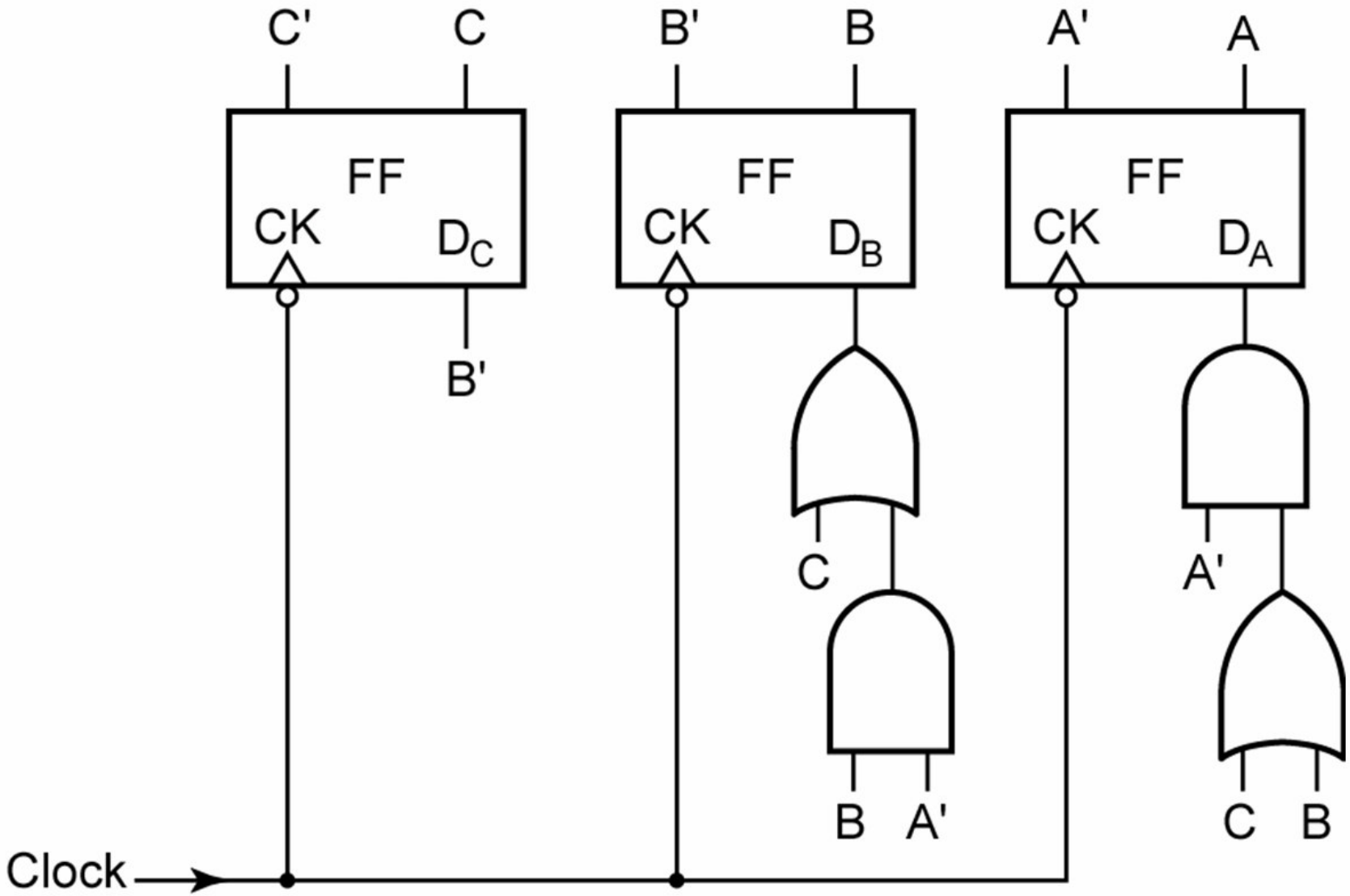


Figure 12-26: **Counter of Figure 12-21 Using D Flip-Flops**

Table 12-5. S-R Flip-Flop Inputs

(a)

S	R	Q	Q^+	
0	0	0	0	
0	0	1	1	
0	1	0	0	
0	1	1	0	
1	0	0	1	
1	0	1	1	
1	1	0	–	inputs not
1	1	1	–	allowed

(b)

Q	Q^+	S	R
0	0	0	0
		0	1
0	1	1	0
1	0	0	1
1	1	0	0
		1	0

(c)

Q	Q^+	S	R
0	0	0	X
0	1	1	0
1	0	0	1
1	1	X	0

$$Q^+ = S + R'Q$$

$(SR = 0)$

Table 12-6.

C	B	A	C^+	B^+	A^+	S_C	R_C	S_B	R_B	S_A	R_A
0	0	0	1	0	0	1	0	0	X	0	X
0	0	1	–	–	–	X	X	X	X	X	X
0	1	0	0	1	1	0	X	X	0	1	0
0	1	1	0	0	0	0	X	0	1	0	1
1	0	0	1	1	1	X	0	1	0	1	0
1	0	1	–	–	–	X	X	X	X	X	X
1	1	0	–	–	–	X	X	X	X	X	X
1	1	1	0	1	0	0	1	X	0	0	1

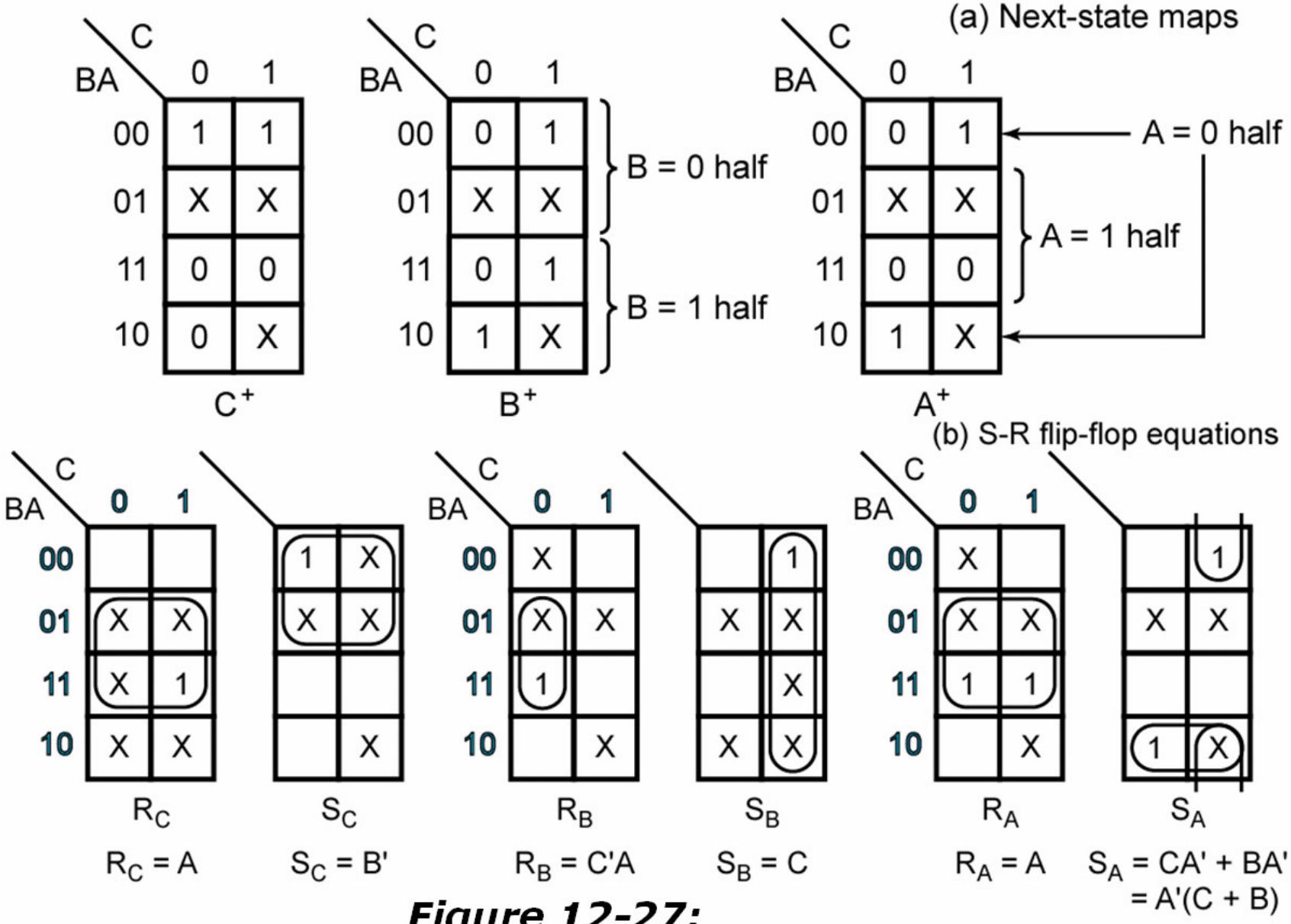
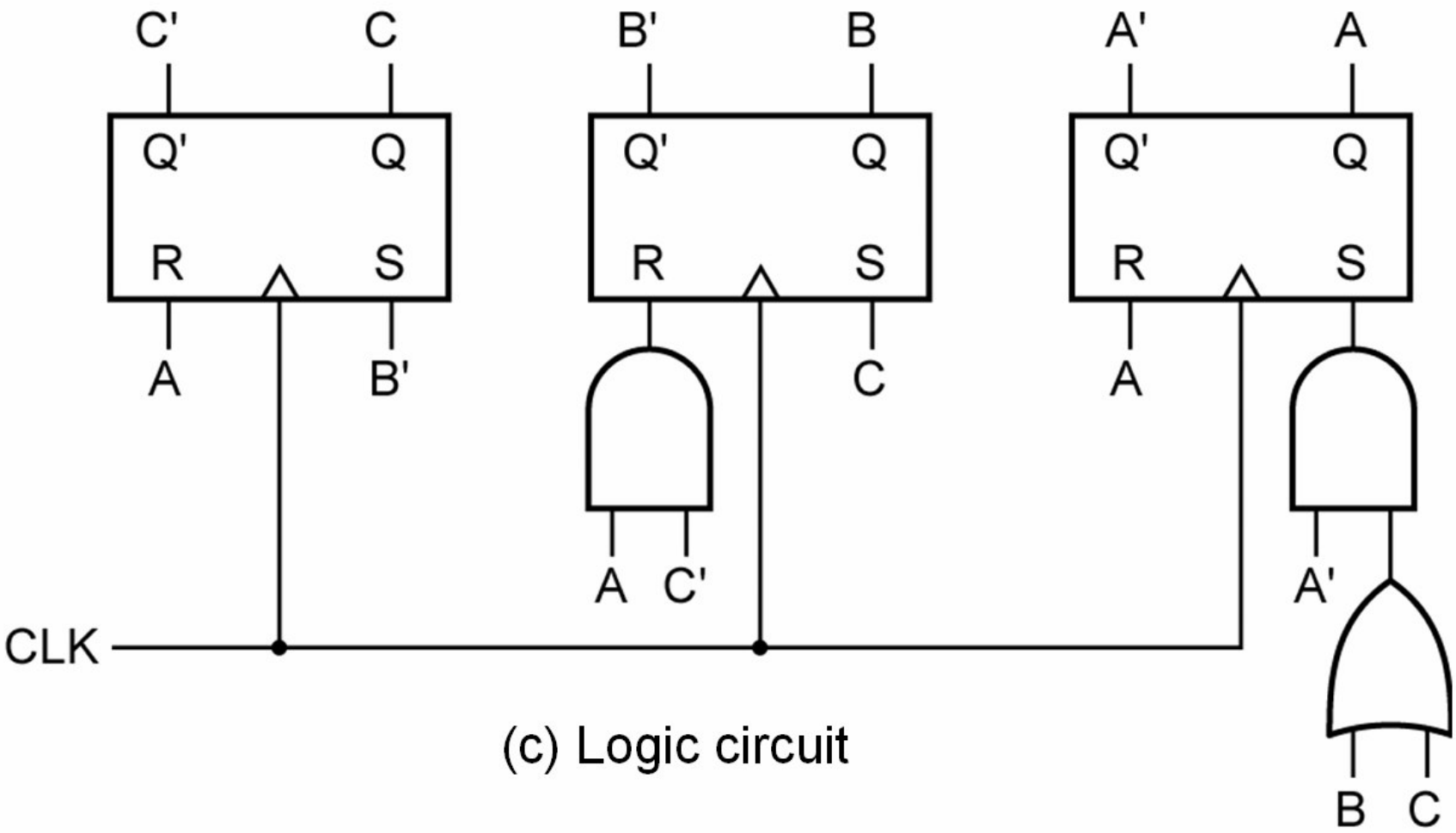


Figure 12-27:
Counter of Figure 12-21 Using S-R Flip-Flops



(c) Logic circuit

Figure 12-27:

Counter of Figure 12-21 Using S-R Flip-Flops

Table 12-7. J-K Flip-Flop Inputs

(a)

J	K	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

(b)

Q	Q^+	J	K
0	0	0	0
		0	1
0	1	1	0
		1	1
1	0	0	1
		1	1
1	1	0	0
		1	0

(c)

Q	Q^+	J	K
0	0	0	X
0	1	1	X
1	0	X	1
1	1	X	0

$$Q^+ = JQ' + K'Q$$

Table 12-8.

C	B	A	C^+	B^+	A^+	J_C	K_C	J_B	K_B	J_A	K_A
0	0	0	1	0	0	1	X	0	X	0	X
0	0	1	–	–	–	X	X	X	X	X	X
0	1	0	0	1	1	0	X	X	0	1	X
0	1	1	0	0	0	0	X	X	1	X	1
1	0	0	1	1	1	X	0	1	X	1	X
1	0	1	–	–	–	X	X	X	X	X	X
1	1	0	–	–	–	X	X	X	X	X	X
1	1	1	0	1	0	X	1	X	0	X	1

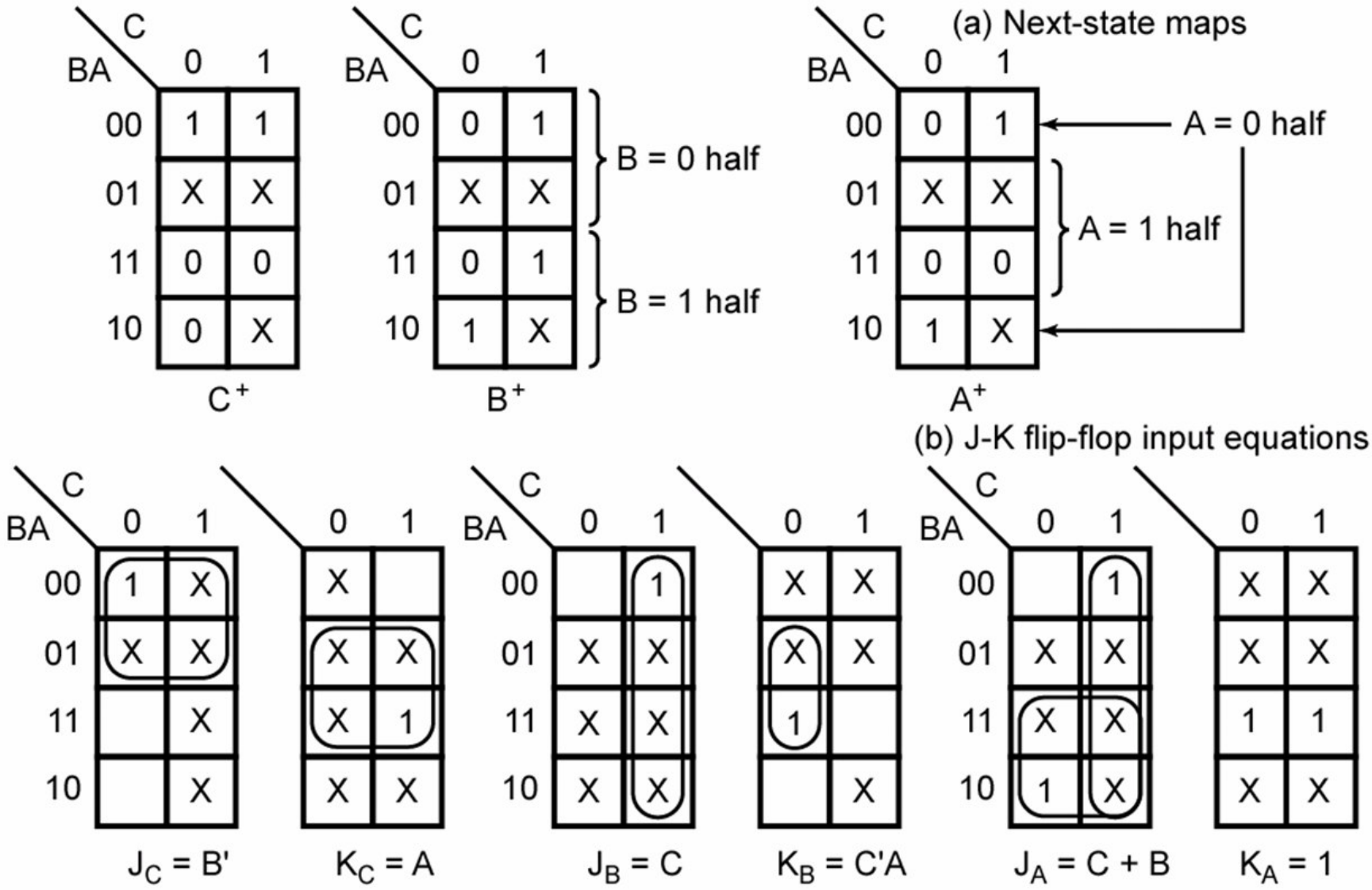
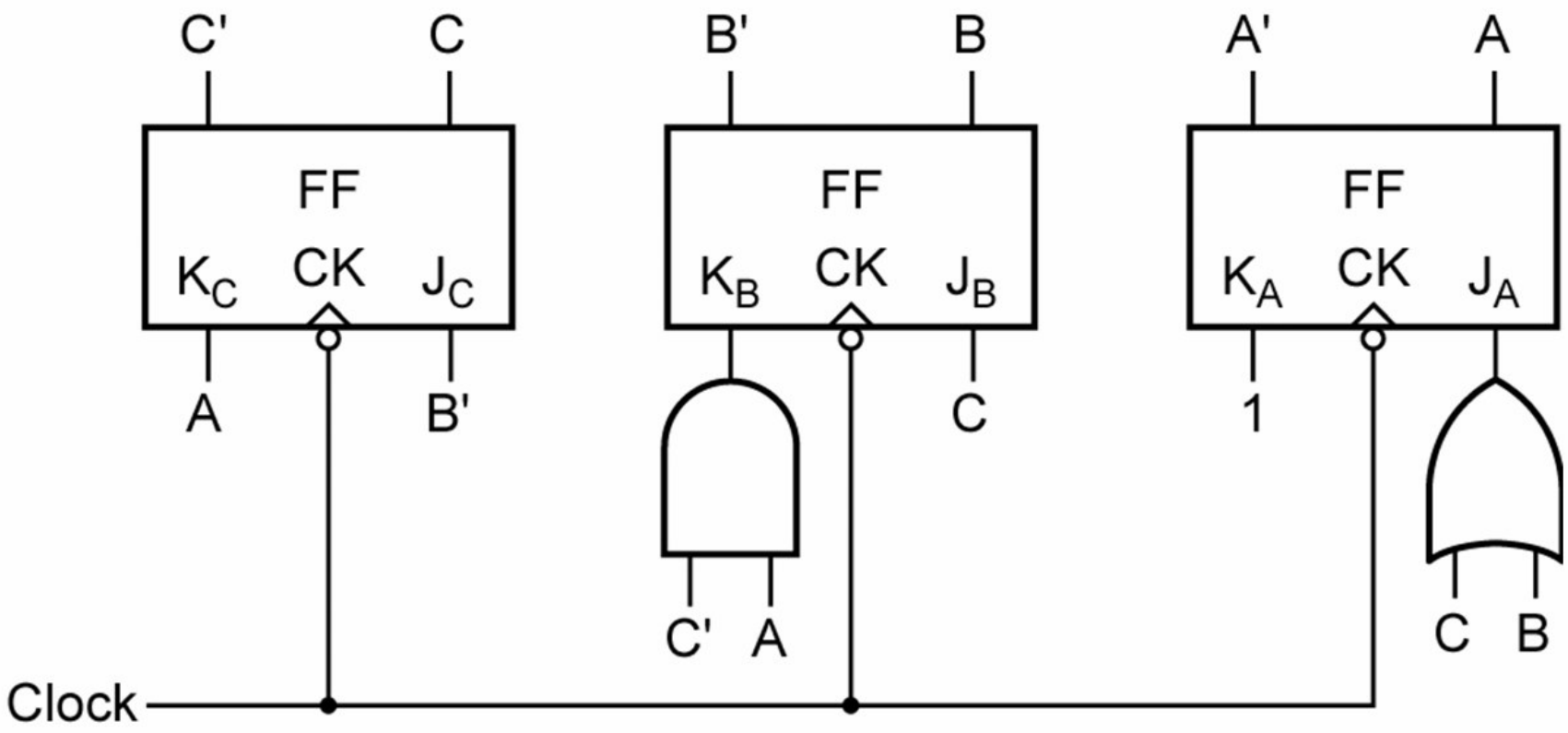


Figure 12-28:
Counter of Figure 12-21 Using J-K Flip-Flops



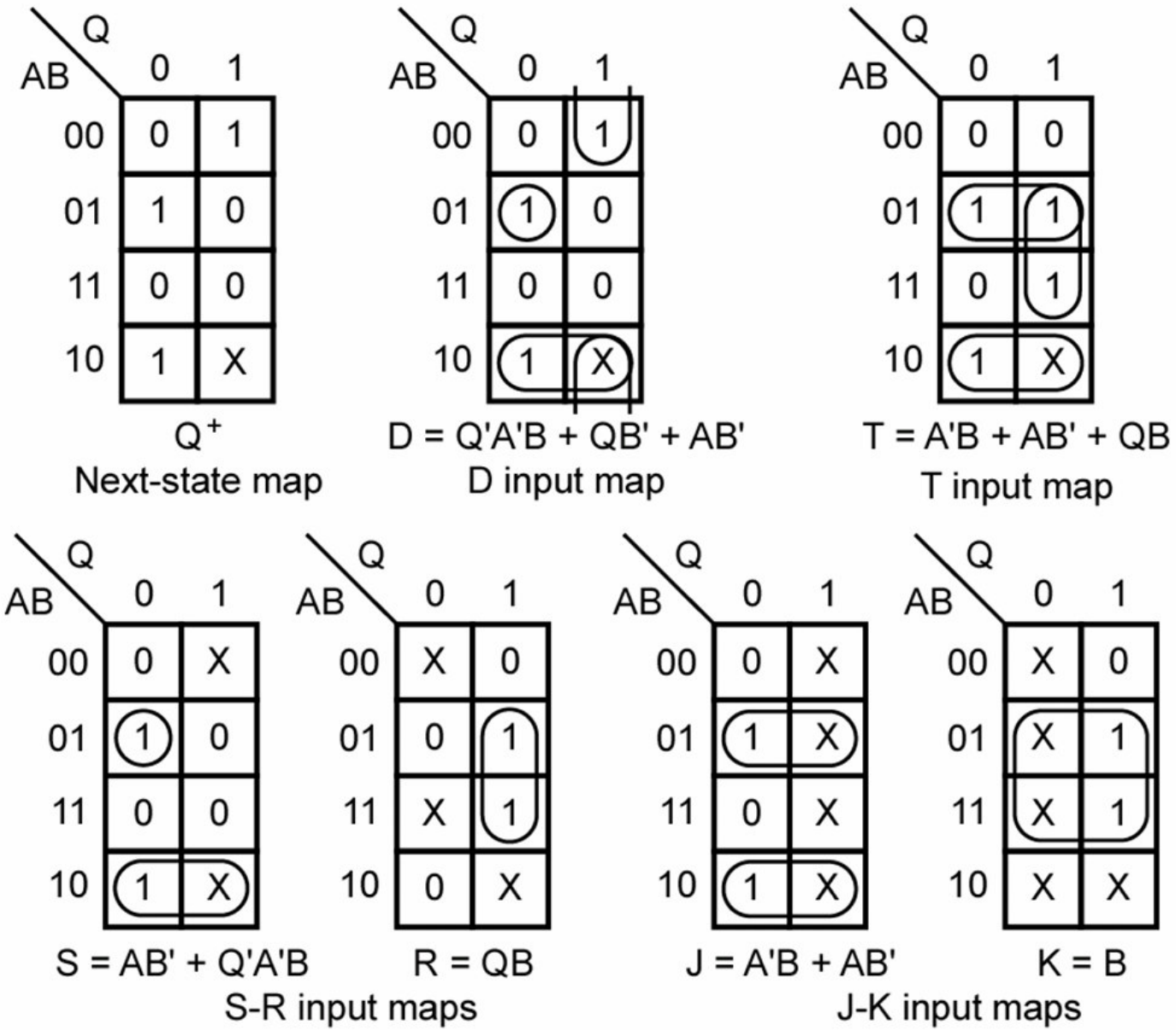
(c) Logic circuit (omitting the feedback lines)

Figure 12-28:

Counter of Figure 12-21 Using J-K Flip-Flops

Table 12-9. Determination of Flip-Flop Input Equations from Next-State Equations Using Karnaugh Maps

Type of Flip-Flop	Input	$Q = 0$		$Q = 1$		Rules for Forming Input Map From Next State Map*	
		$Q^+ = 0$	$Q^+ = 1$	$Q^+ = 0$	$Q^+ = 1$	$Q = 0$ Half of Map	$Q = 1$ Half of Map
Delay	D	0	1	0	1	no change	no change
Trigger	T	0	1	1	0	no change	complement
Set-Reset	S	0	1	0	X	no change	replace 1's with X's**
	R	X	0	1	0	replace 0's with X's**	complement
J-K	J	0	1	X	X	no change	fill in with X's
	K	X	X	1	0	fill in with X's	complement



Example Illustrating the Use of Table 12-9

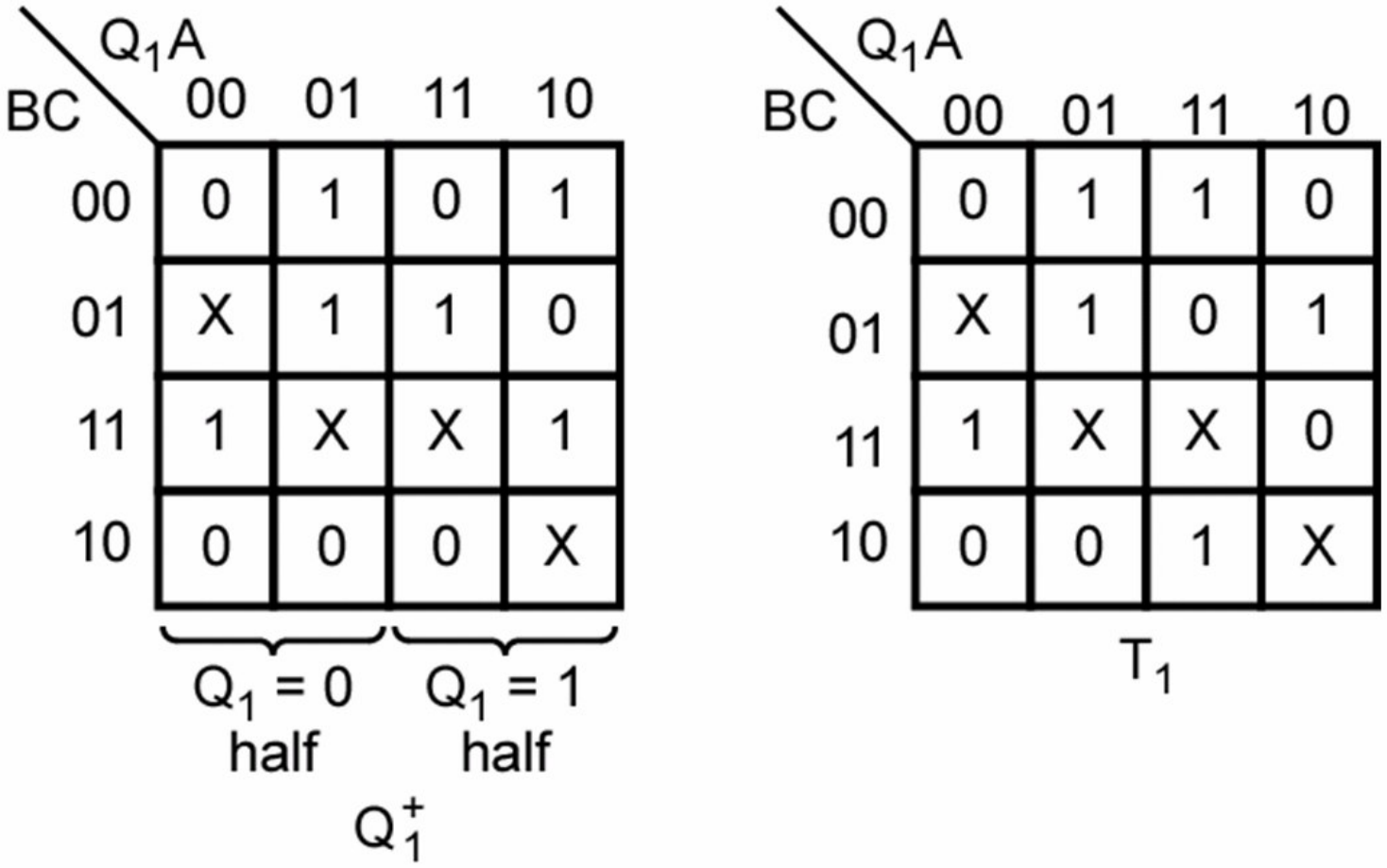


Figure 12-29a:
Derivation of Flip-Flop Input Equations Using 4-Variable Maps

Figure 12-29b:
Derivation of Flip-Flop Input Equations Using 4-Variable Maps

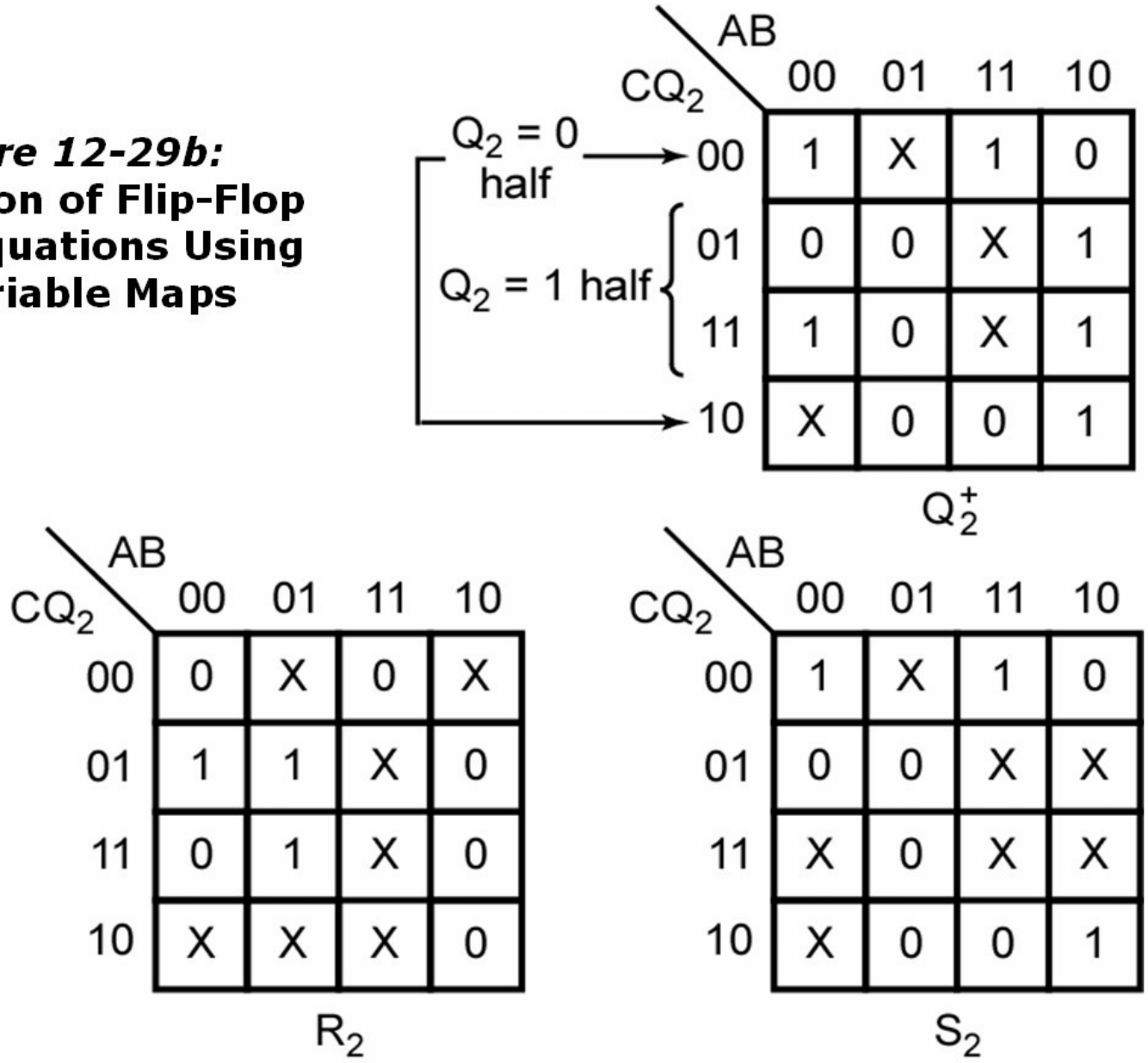


Figure 12-29c:
Derivation of Flip-Flop Input Equations Using 4-Variable Maps