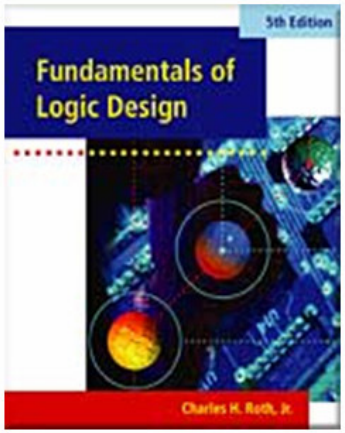
FIGURES FOR

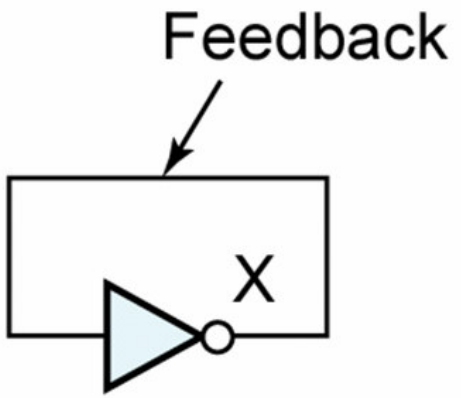
CHAPTER 11

LATCHES AND FLIP-FLOPS

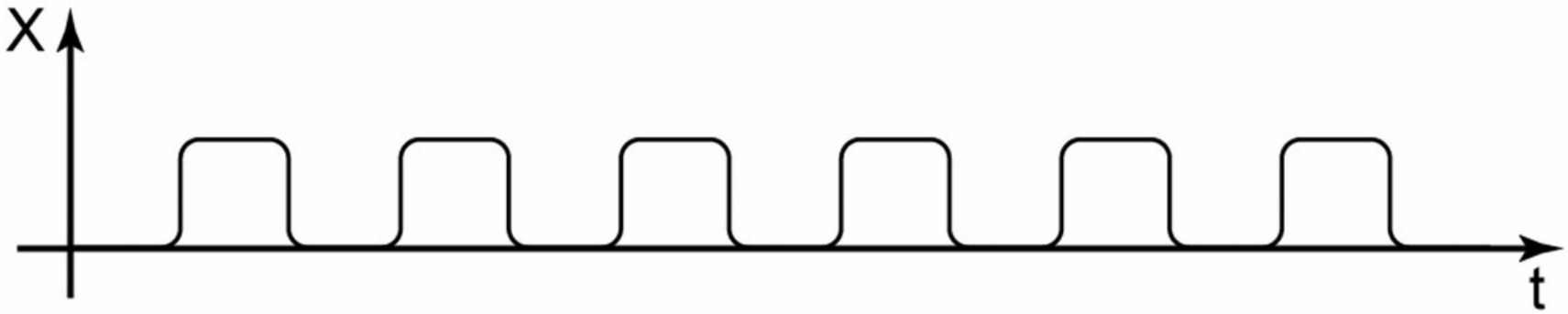


This chapter in the book includes:

Click the mouse to move to the next page.
Use the ESC key to exit this chapter.

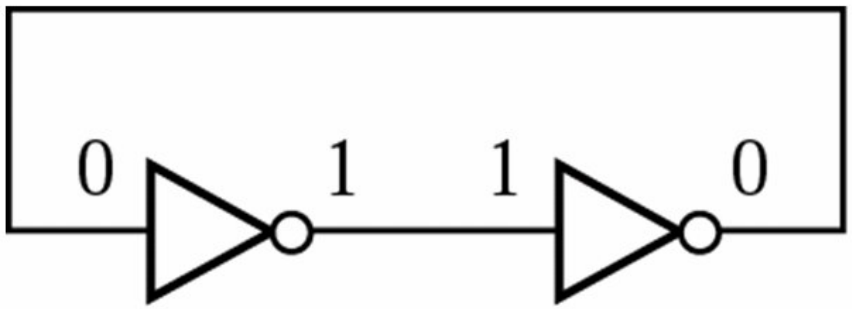


(a) Inverter with feedback

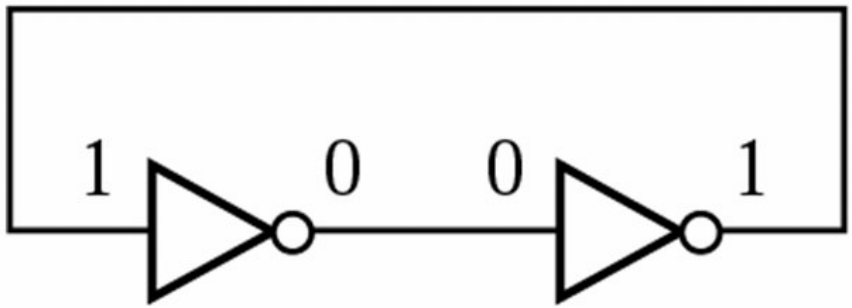


(b) Oscillation at inverter output

Figure 11-1

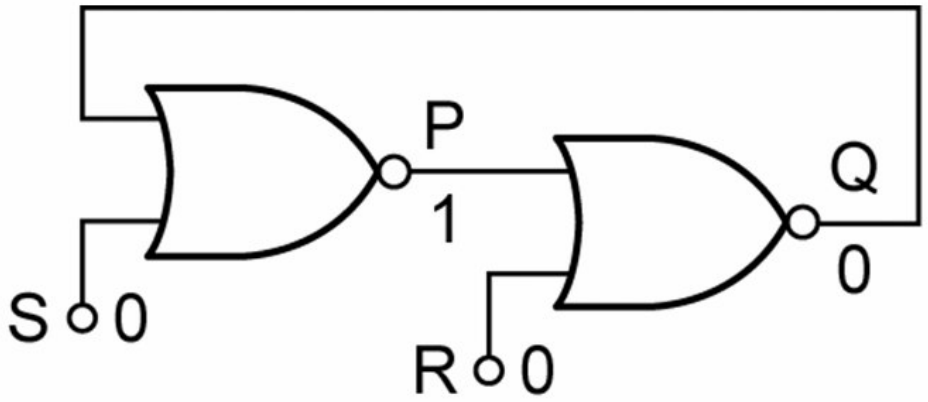


(a)

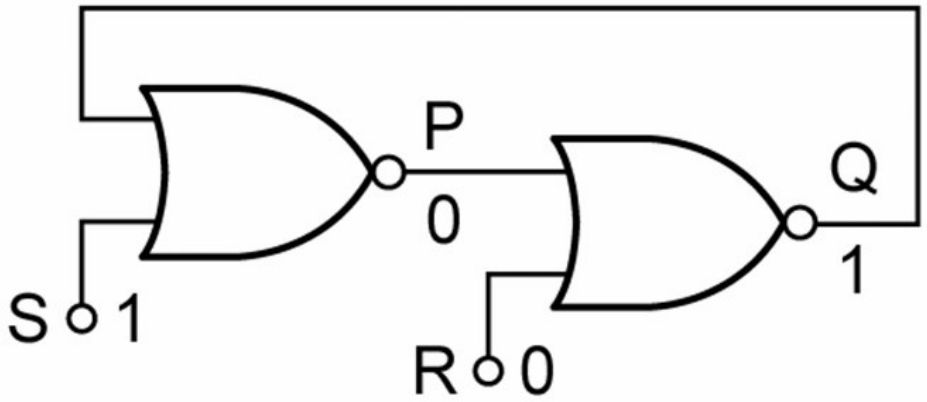


(b)

Figure 11-2

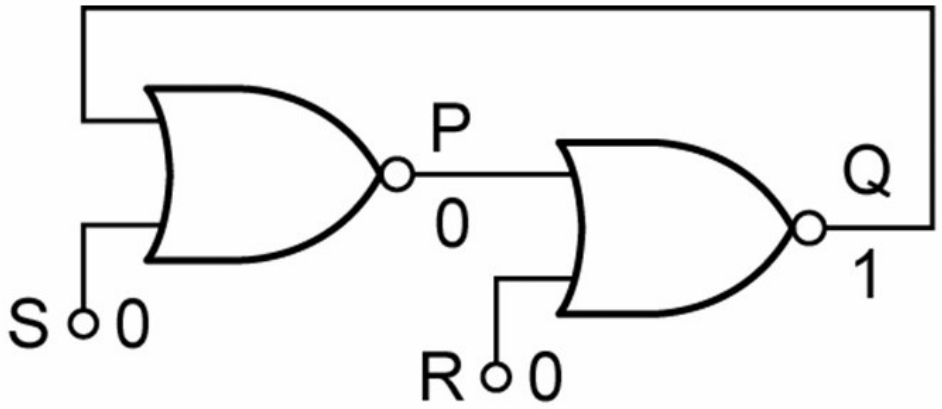


(a)

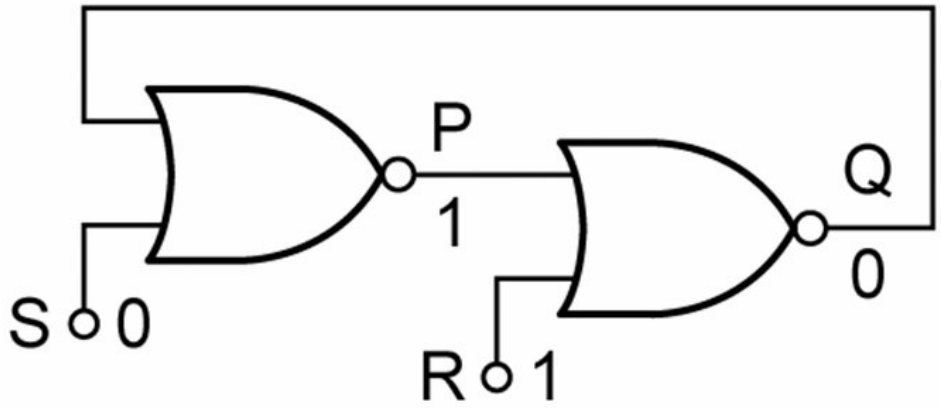


(b)

Figure 11-3



(a)



(b)

Figure 11-4

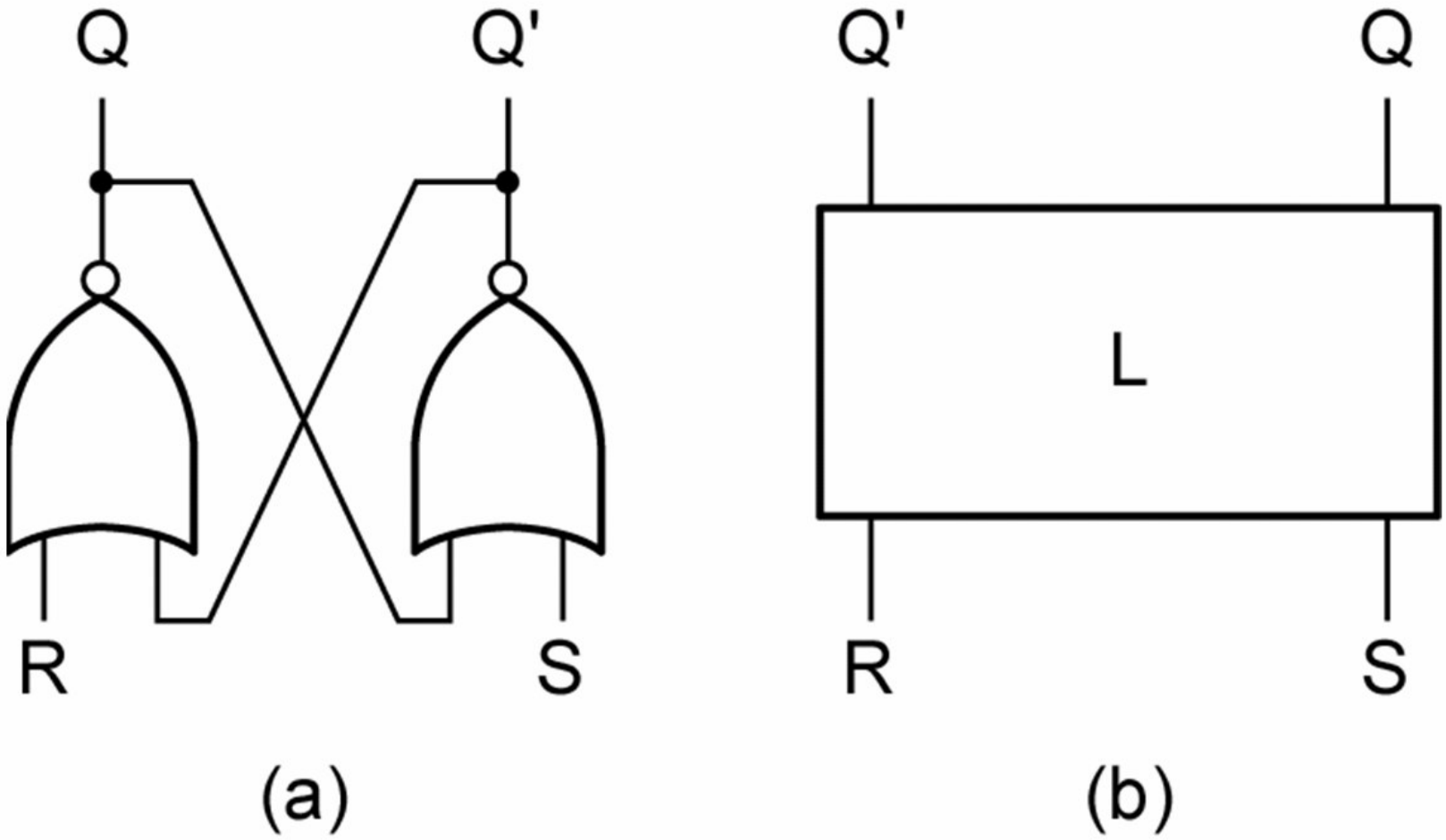


Figure 11-5: **S-R Latch**

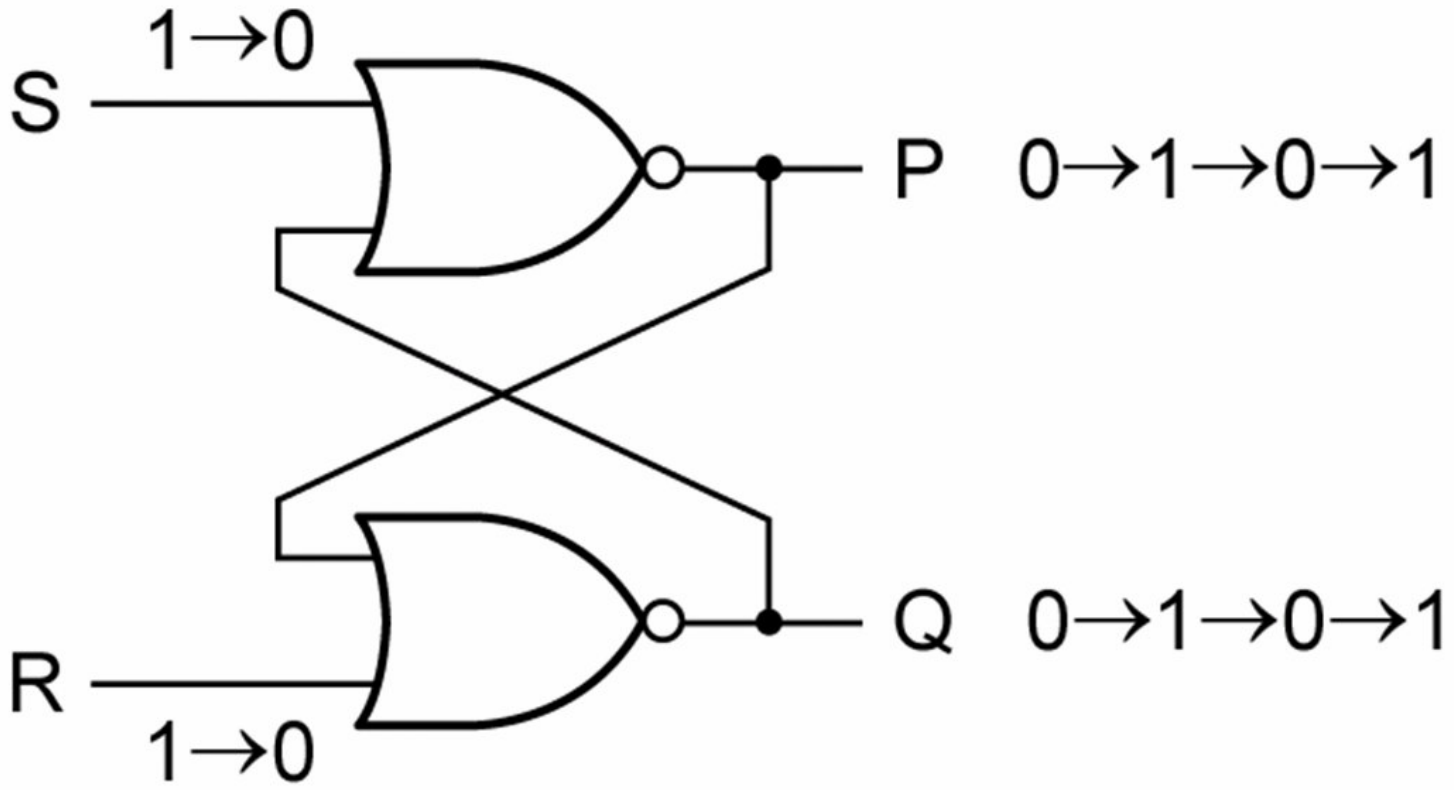


Figure 11-6: **Improper S-R Latch Operation**

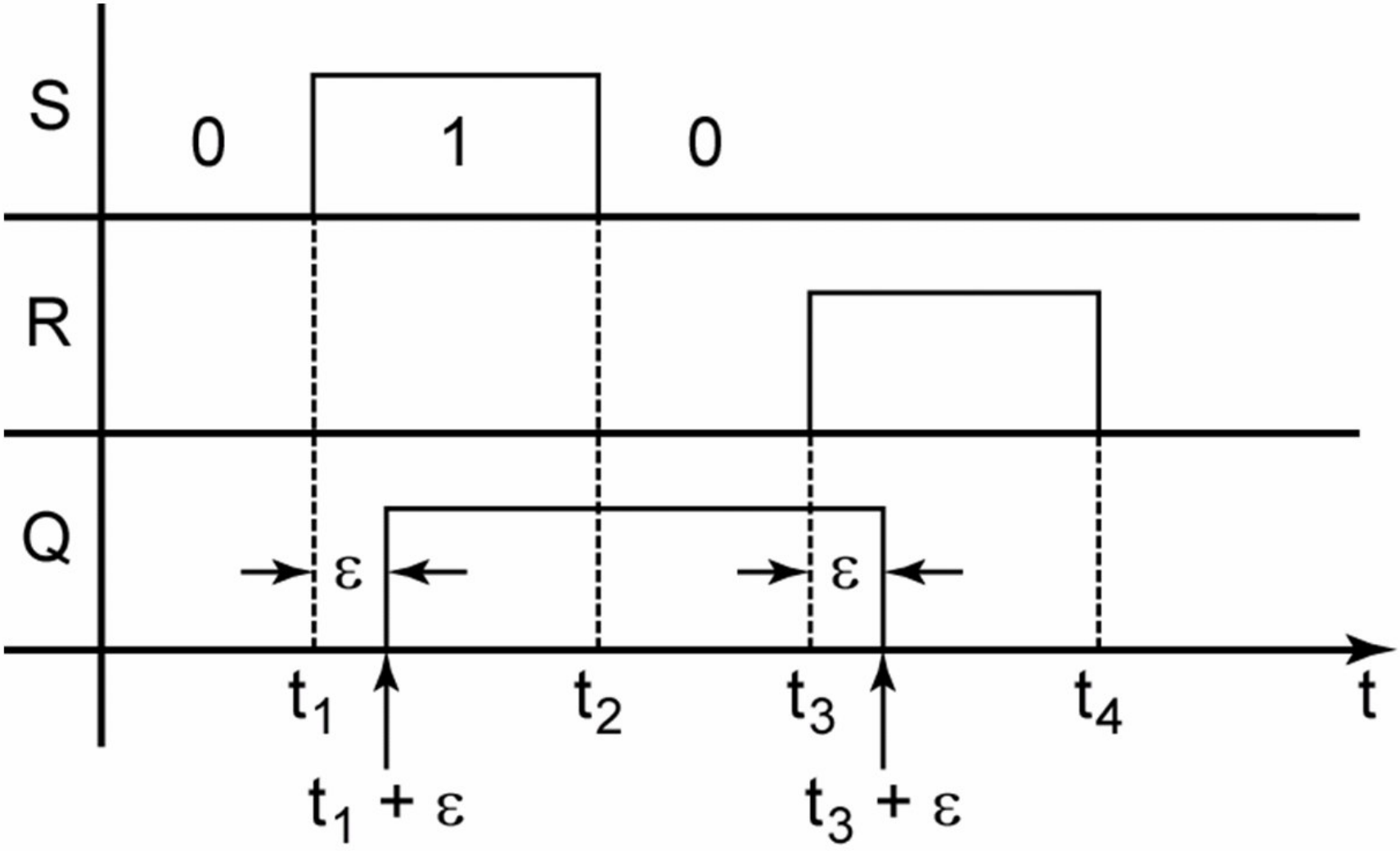
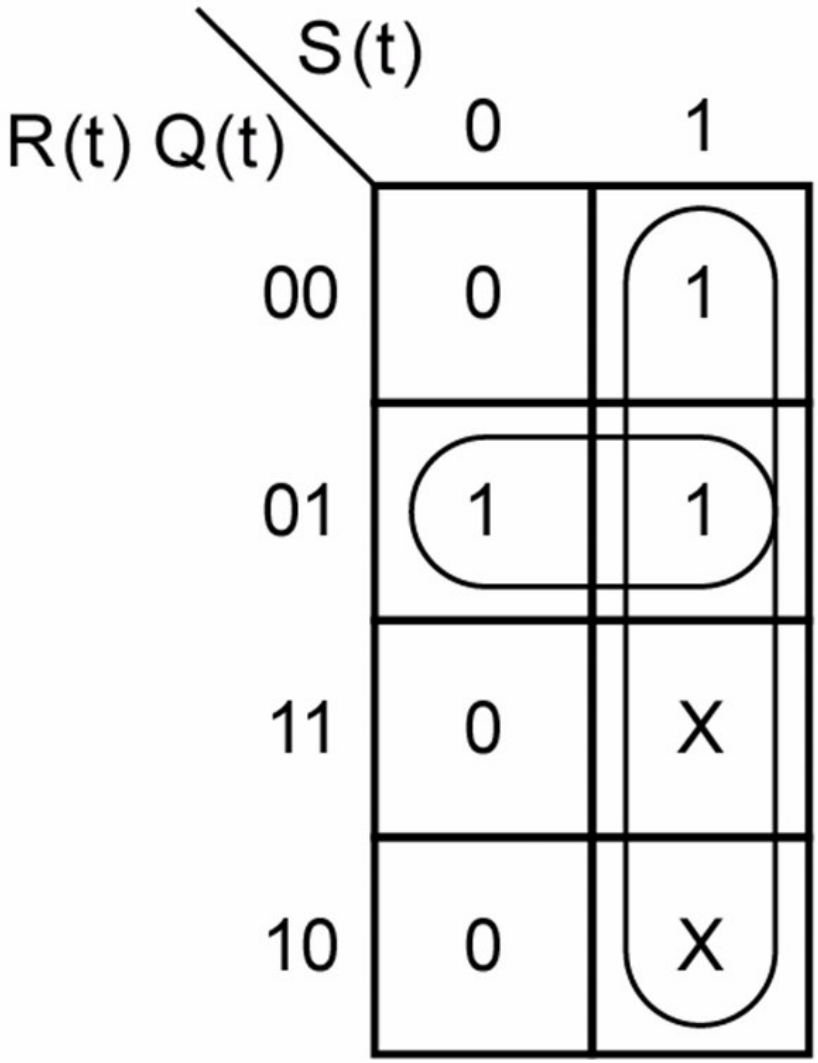


Figure 11-7: **Timing Diagram for S-R Latch**

$S(t)$	$R(t)$	$Q(t)$	$Q(t+\epsilon)$	
0	0	0	0	
0	0	1	1	
0	1	0	0	
0	1	1	0	
1	0	0	1	
1	0	1	1	
1	1	0	—	} inputs not allowed
1	1	1	—	

Table 11-1. S-R Latch Operation



$$Q(t + \varepsilon) = S(t) + R'(t)\,Q(t)$$

Figure 11-8: **Map for $Q(t + \varepsilon)$**

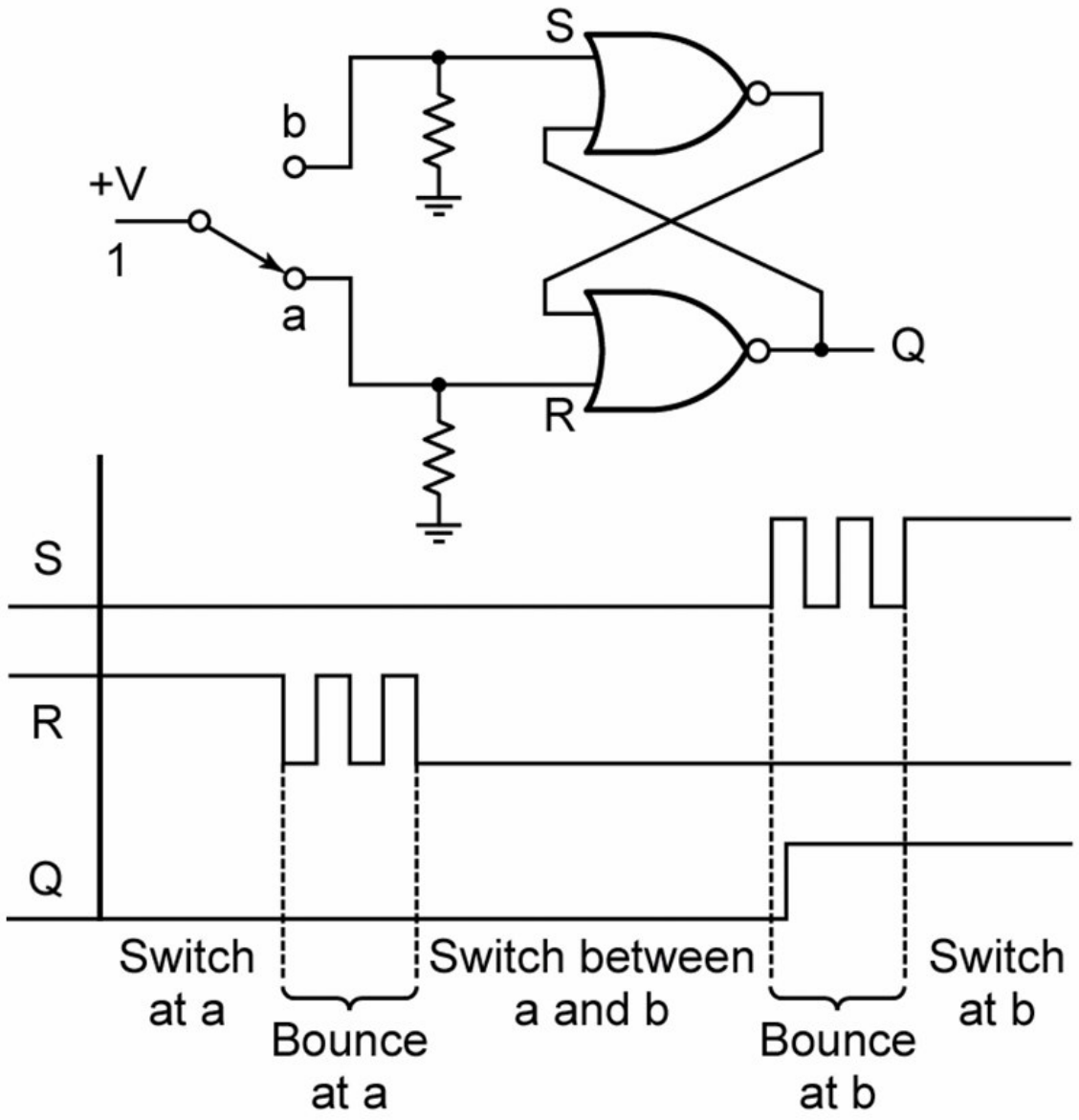
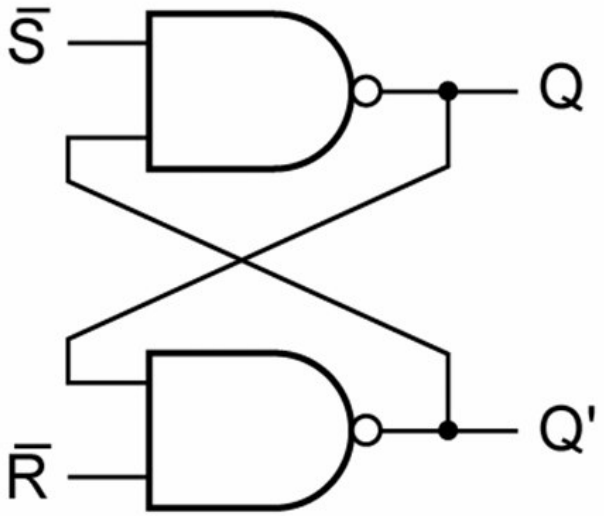
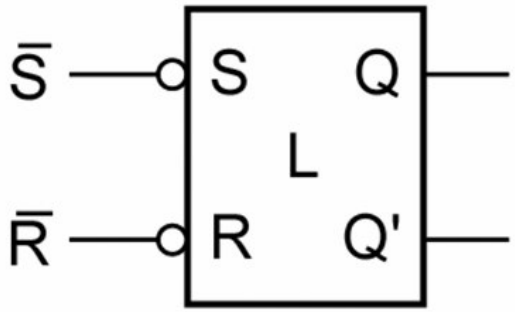


Figure 11-9: **Switch Debouncing with an S-R Latch**



(a)



(b)

$\bar{S}$	$\bar{R}$	Q	Q^+	
1	1	0	0	
1	1	1	1	
1	0	0	0	
1	0	1	0	
0	1	0	1	
0	1	1	1	
0	0	0	–	inputs not allowed
0	0	1	–	

Figure 11-10: **$\bar{S}$-$\bar{R}$ Latch**

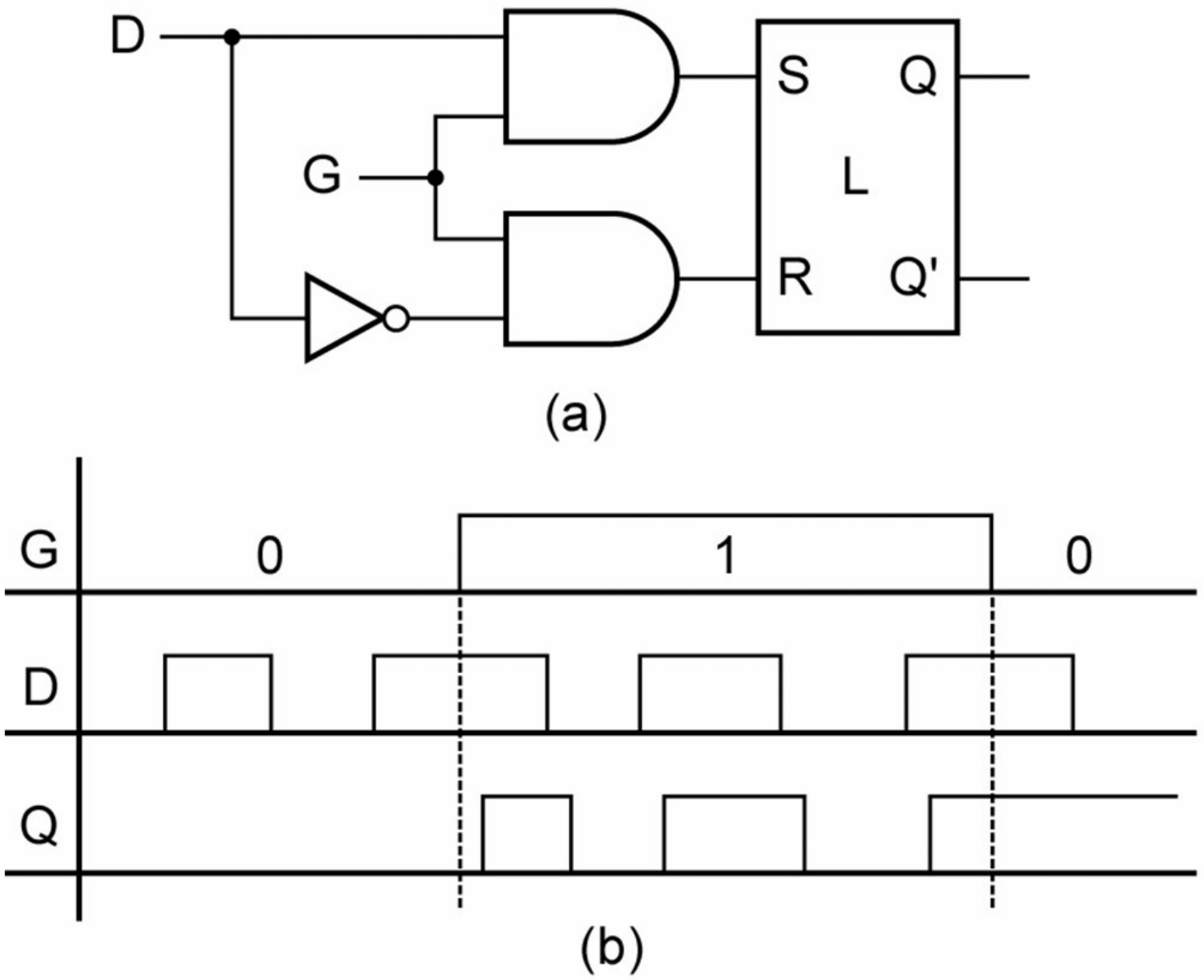
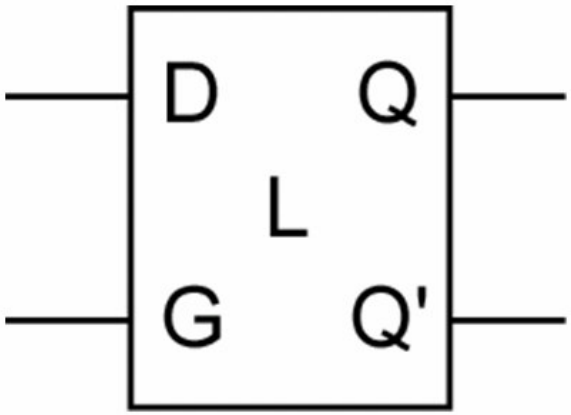


Figure 11-11: **Gated D Latch**



G	D	Q	Q^+
0	0	0	0
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Figure 11-12 (left): **Symbol and Truth Table for Gated Latch**

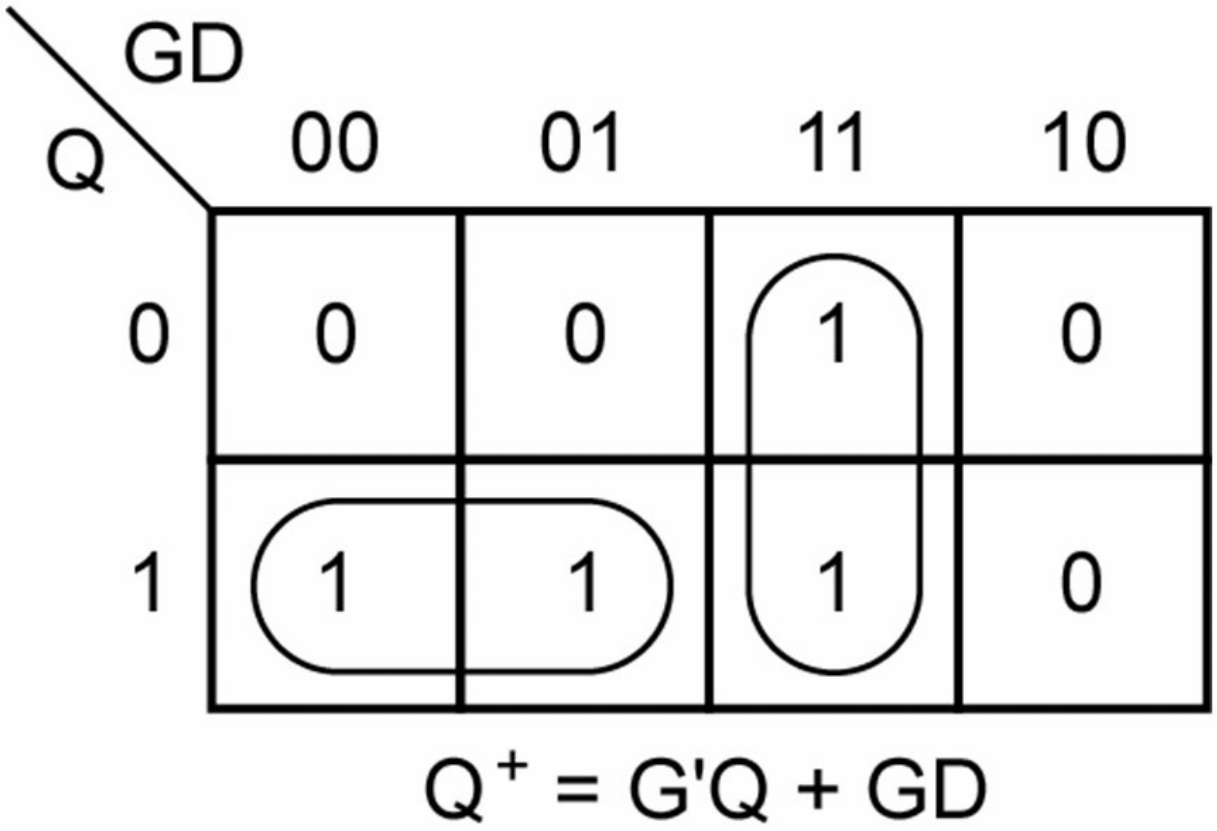
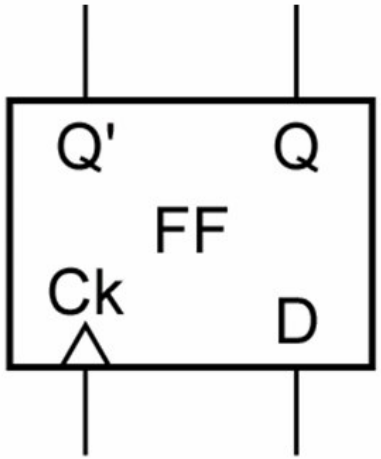
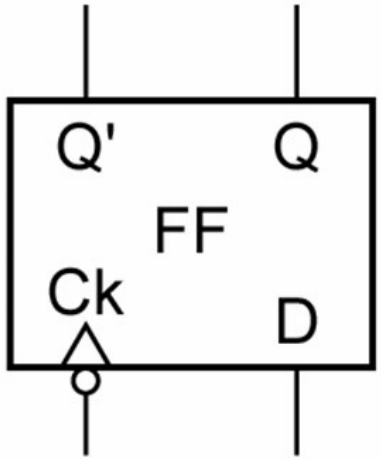


Figure 11-12 (continued)



(a) Rising-edge trigger



(b) Falling-edge trigger

D	Q	Q^+
0	0	0
0	1	0
1	0	1
1	1	1

(c) truth table

$$Q^+ = D$$

Figure 11-13: **D Flip-Flops**

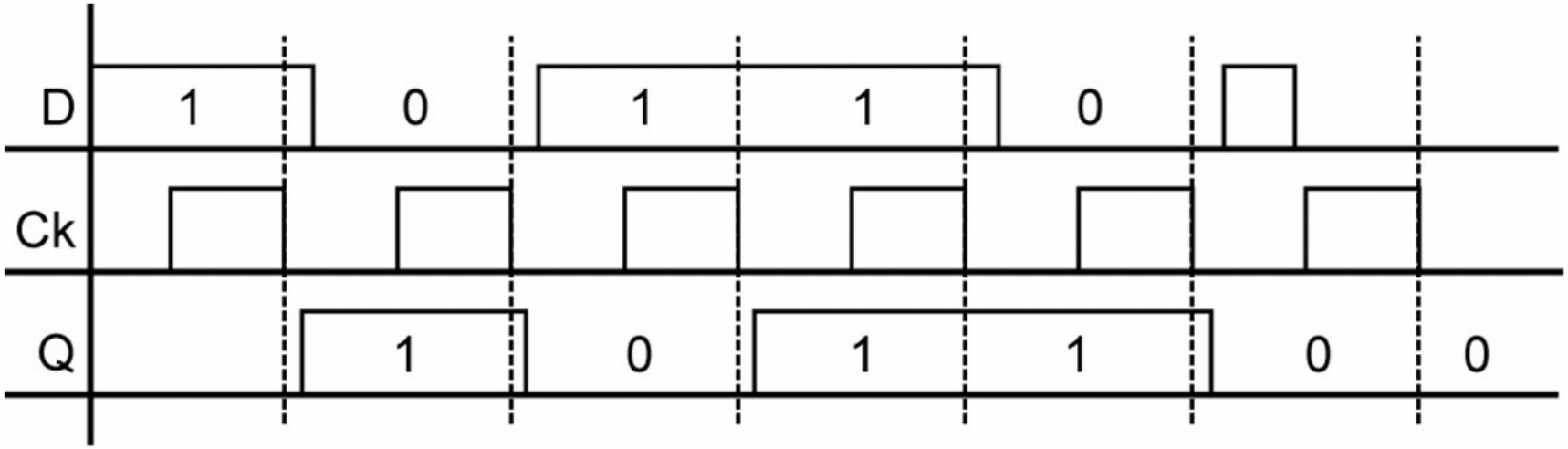
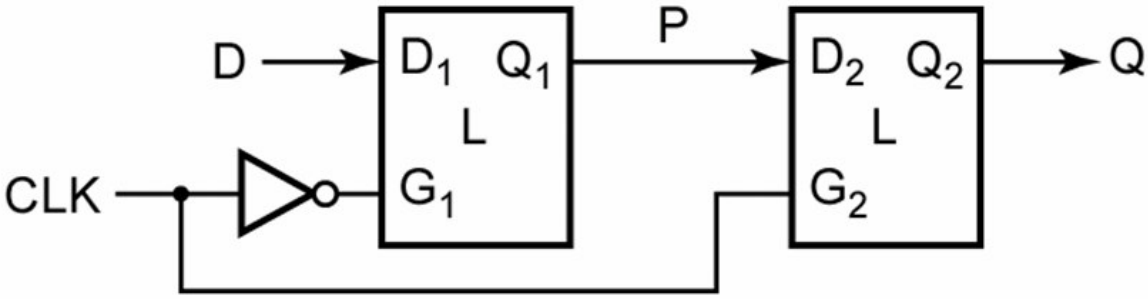
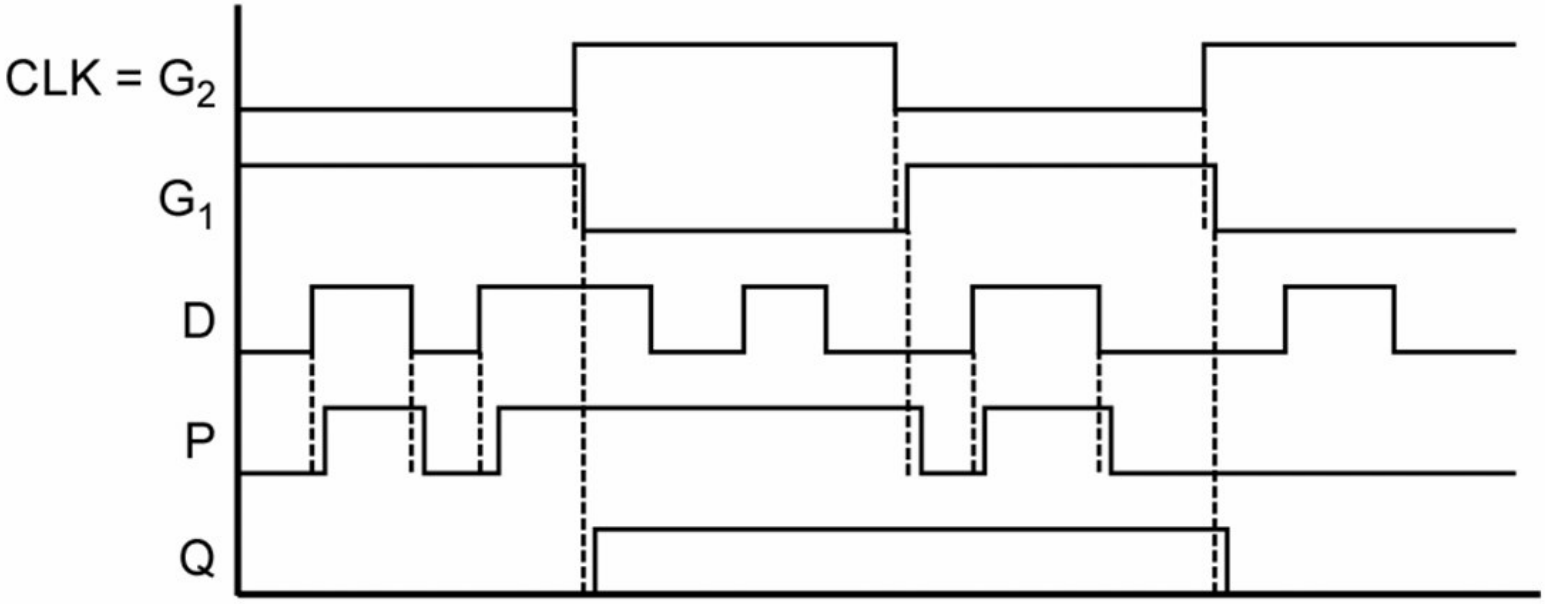


Figure 11-14: **Timing for D Flip-Flop (Falling Edge Trigger)**



(a) Construction from two gated D latches



(b) Time analysis

Figure 11-15: **D Flip-Flop (Rising Edge Trigger)**

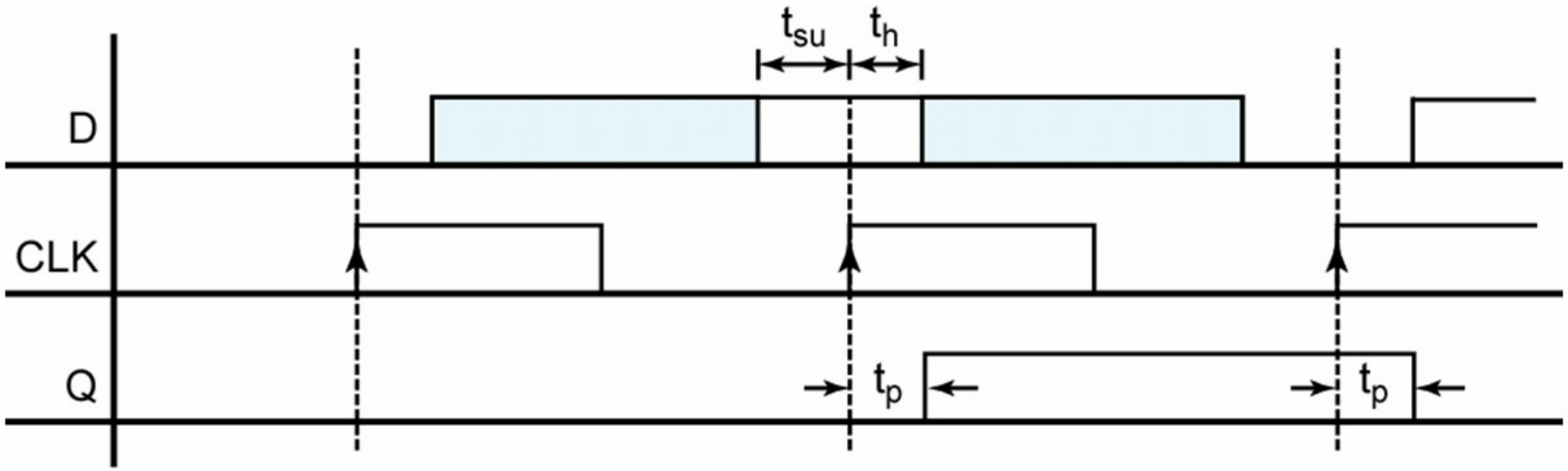


Figure 11-16: **Setup and Hold Times for an Edge-Triggered D Flip-Flop**

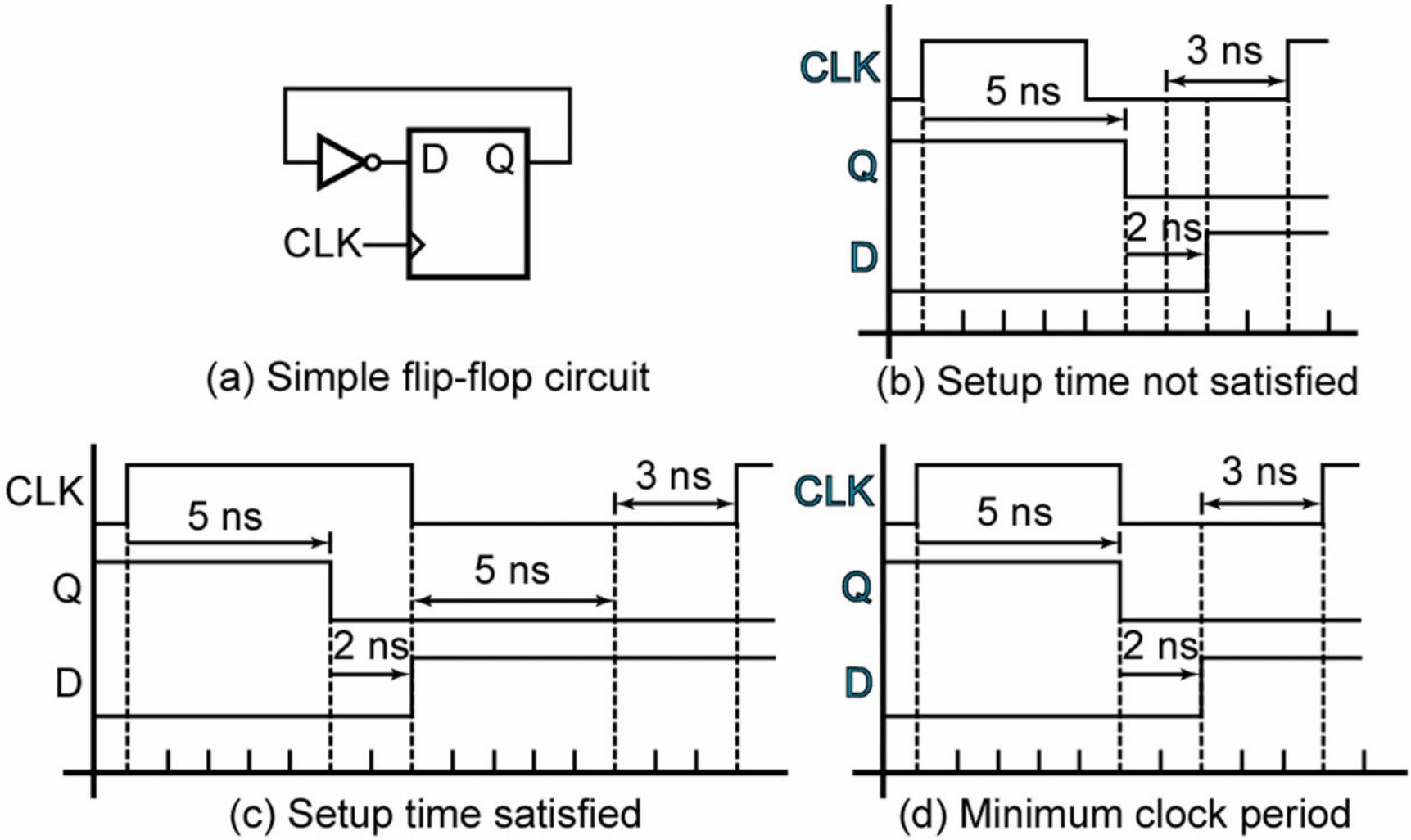
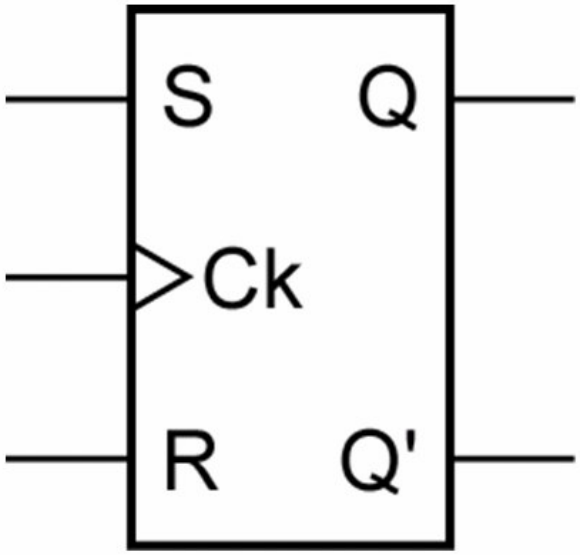


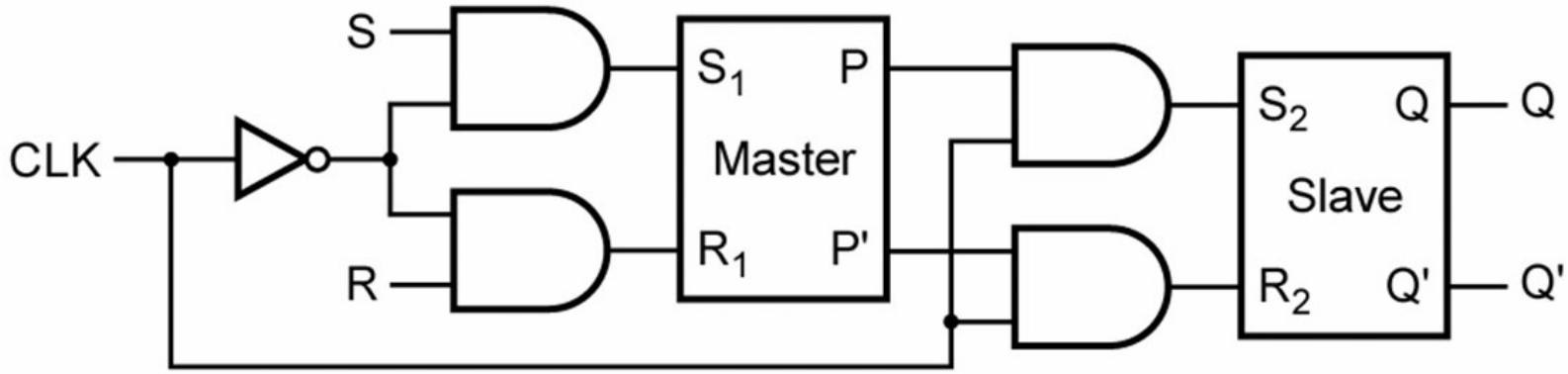
Figure 11-17: **Determination of Minimum Clock Period**



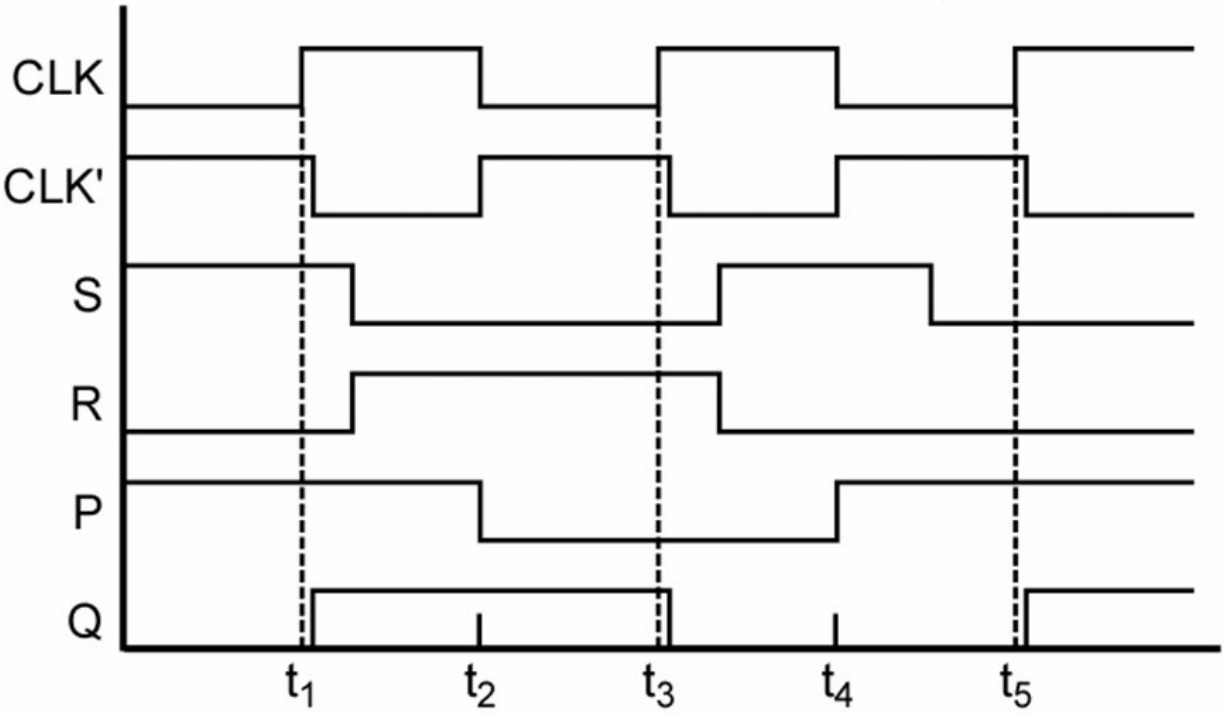
Operation summary:

S = R = 0	no state change
S = 1, R = 0	set Q to 1 (after active Ck edge)
S = 0, R = 1	reset Q to 0 (after active Ck edge)
S = R = 1	not allowed

Figure 11-18: **S-R Flip-Flop**

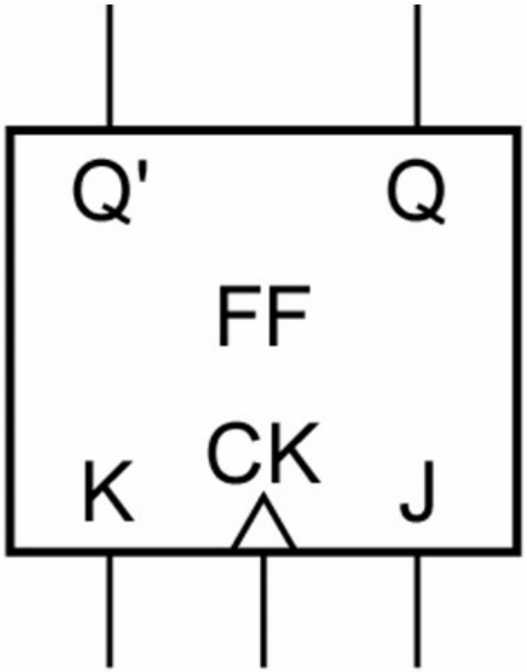


(a) Implementation with two latches



(b) Timing analysis

Figure 11-19: **S-R Flip-Flop Implementation and Timing**



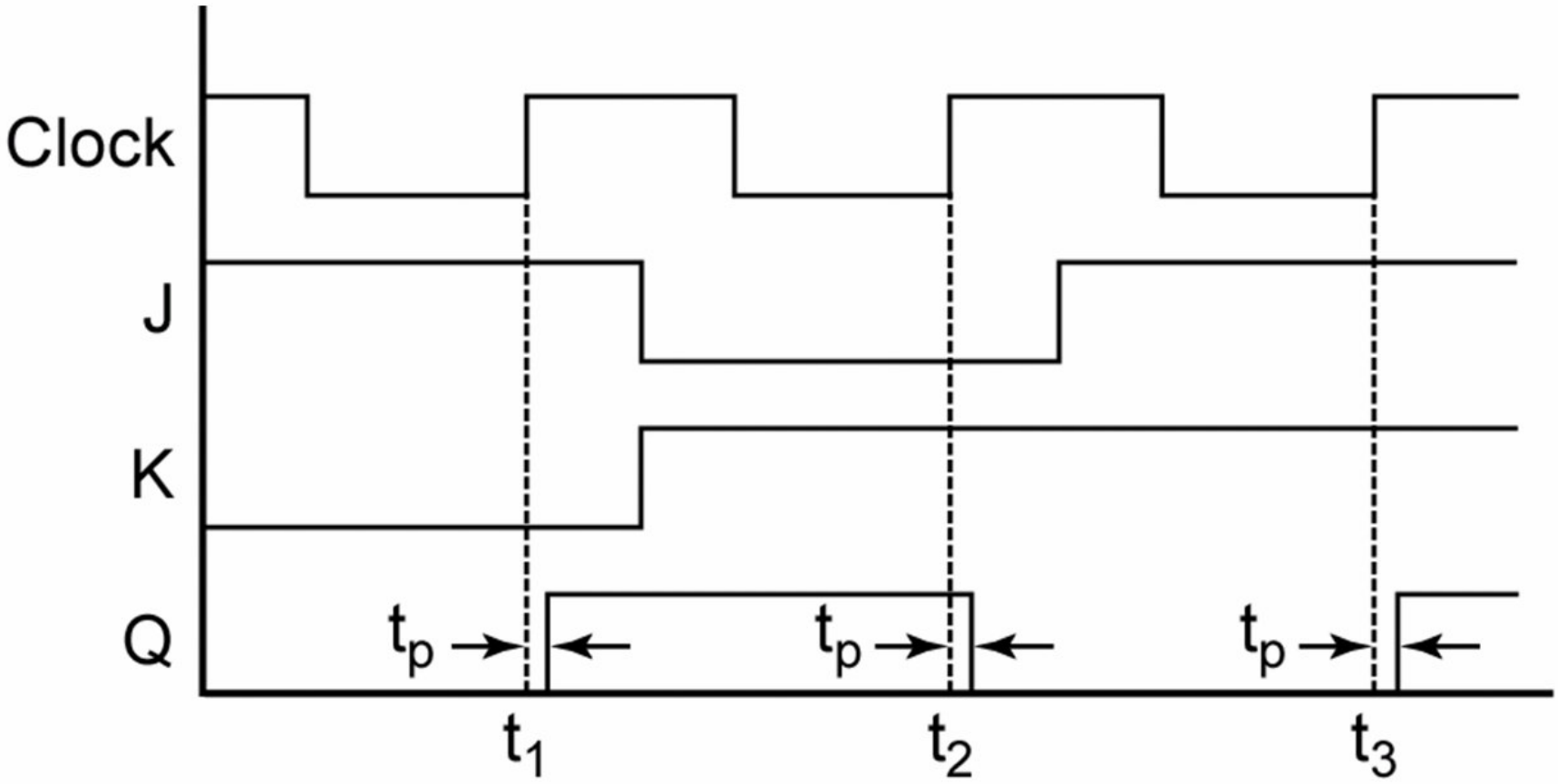
(a) J-K flip-flop

$$Q^+ = JQ' + K'Q$$

(b)

JKQ	Q^+
000	0
001	1
010	0
011	0
100	1
101	1
110	1
111	0

Figure 11-20ab: **J-K Flip-Flop (*Q* Changes on the Rising Edge)**



(c) J-K flip-flop timing

Figure 11-20c: **J-K Flip-Flop (*Q* Changes on the Rising Edge)**

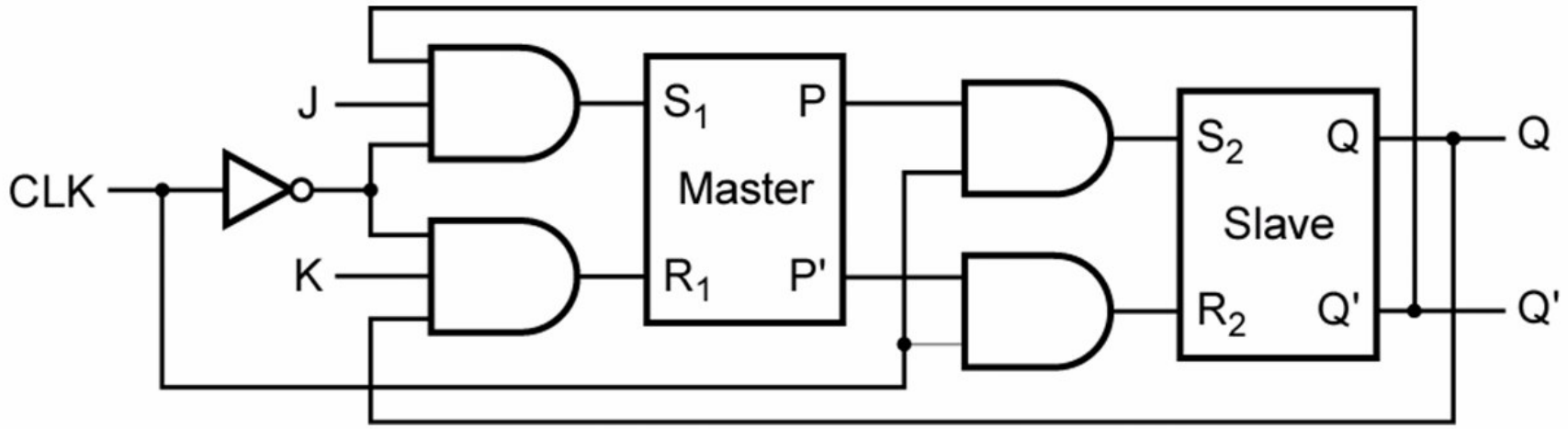
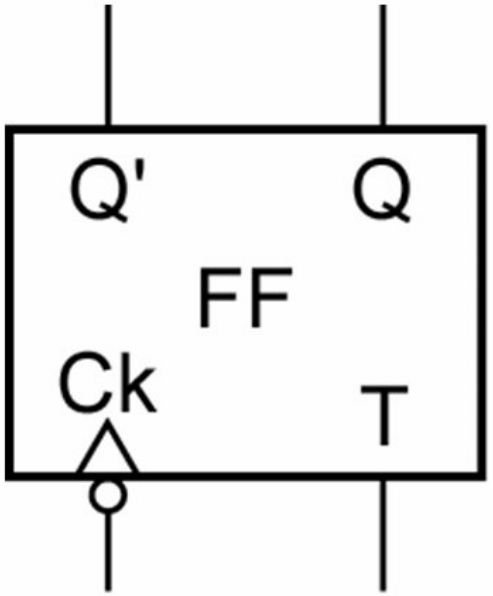


Figure 11-21: **Master-Slave J-K Flip-Flop (*Q* Changes on Rising Edge)**



(a)

(b)

T	Q	Q^+
0	0	0
0	1	1
1	0	1
1	1	0

$$Q^+ = T'Q + TQ' = Q \oplus T$$

Figure 11-22ab: **T Flip-Flop**

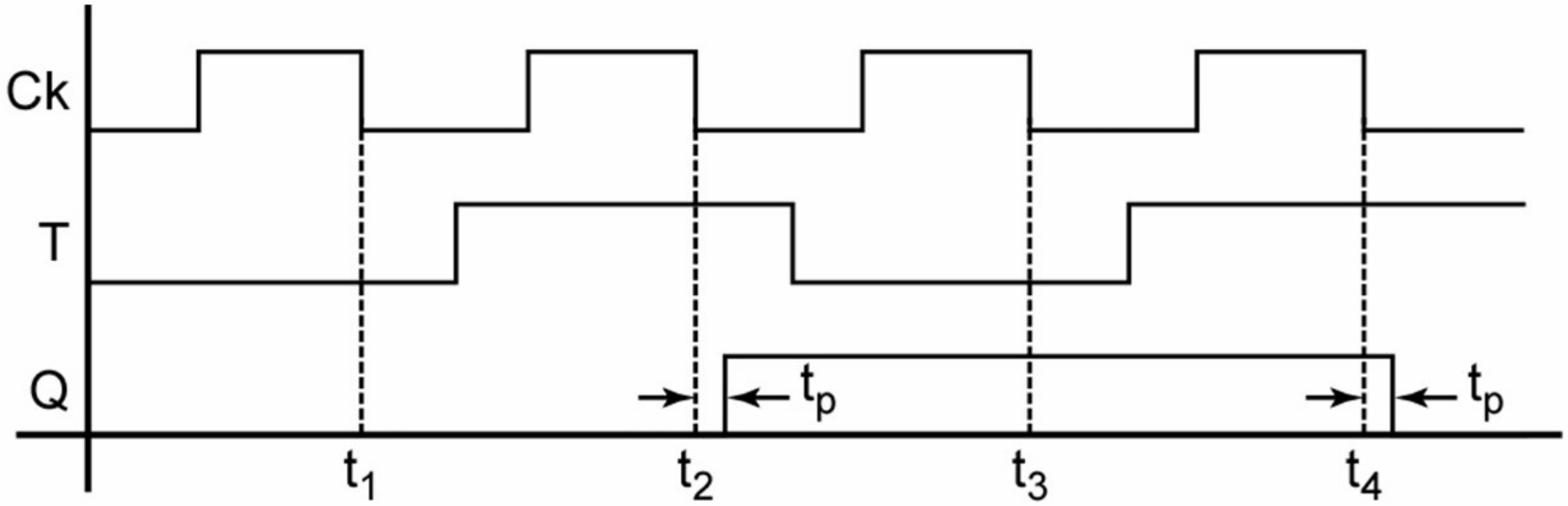
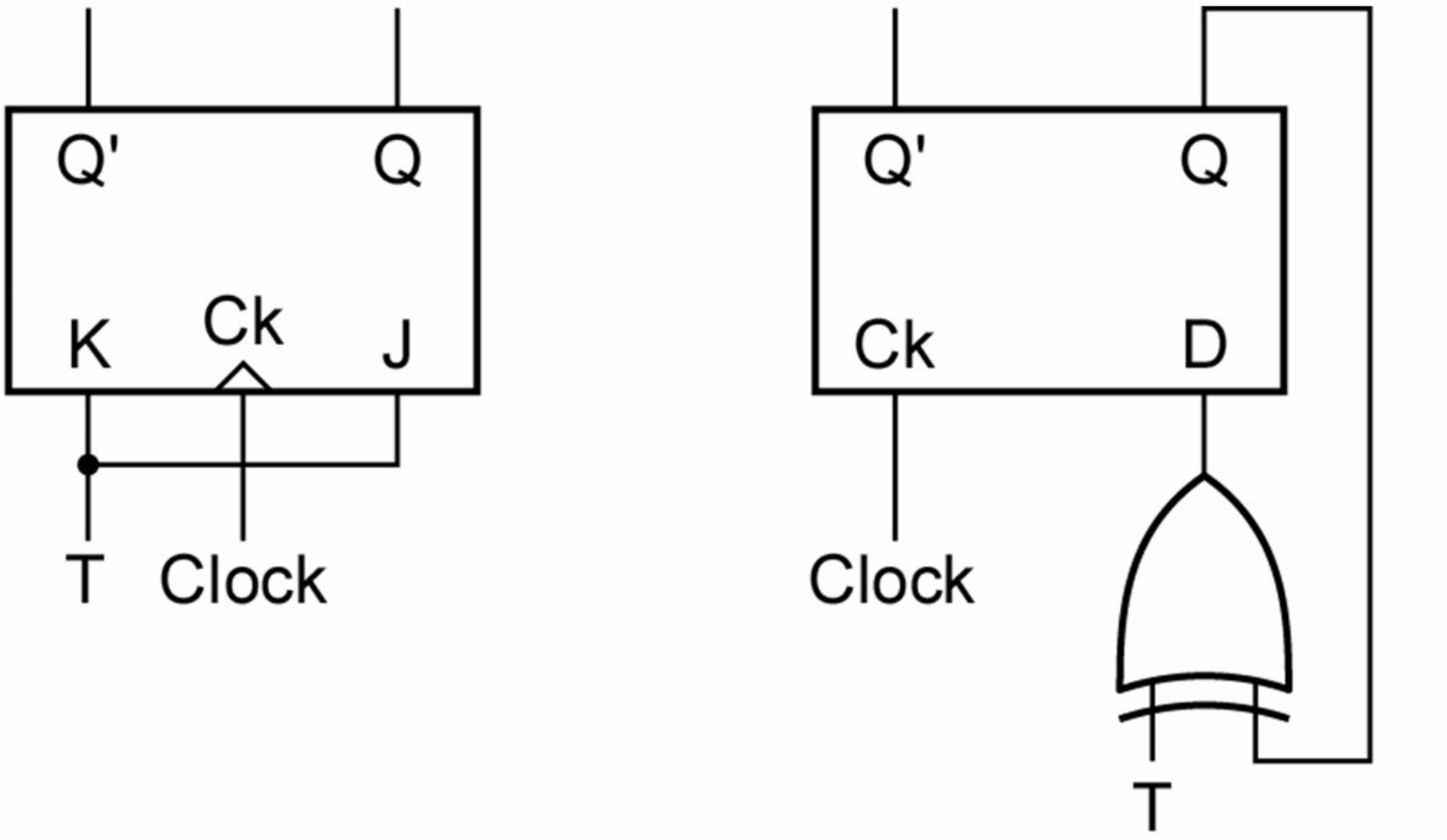
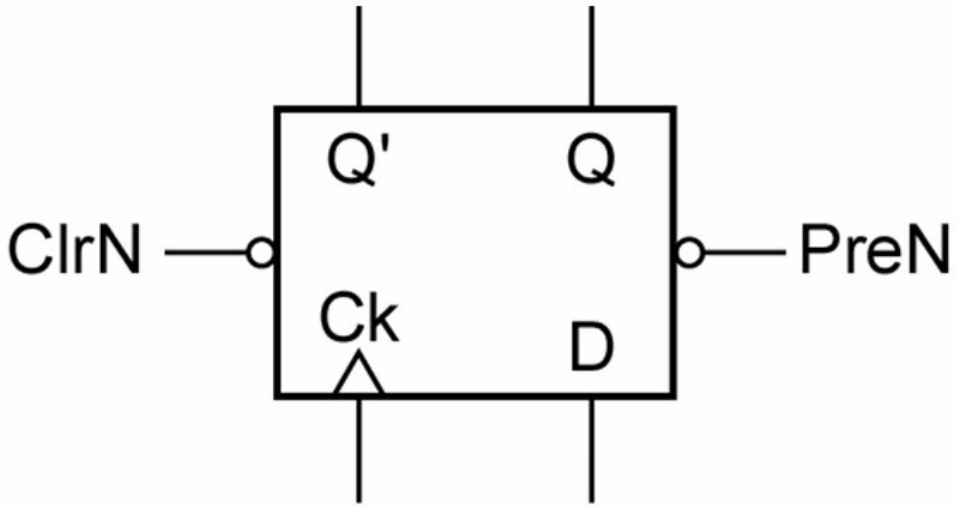


Figure 11-23: **Timing Diagram for T Flip-Flop (Falling-Edge Trigger)**



(a) Conversion of J-K to T (b) Conversion of D to T

Figure 11-24: **Implementation of T Flip-Flops**



CK	D	PreN	ClrN	Q^+
x	x	0	0	(not allowed)
x	x	0	1	1
x	x	1	0	0
↑	0	1	1	0
↑	1	1	1	1
0,1, ↓	x	1	1	Q (no change)

Figure 11-25: **D Flip-Flop with Clear and Preset**

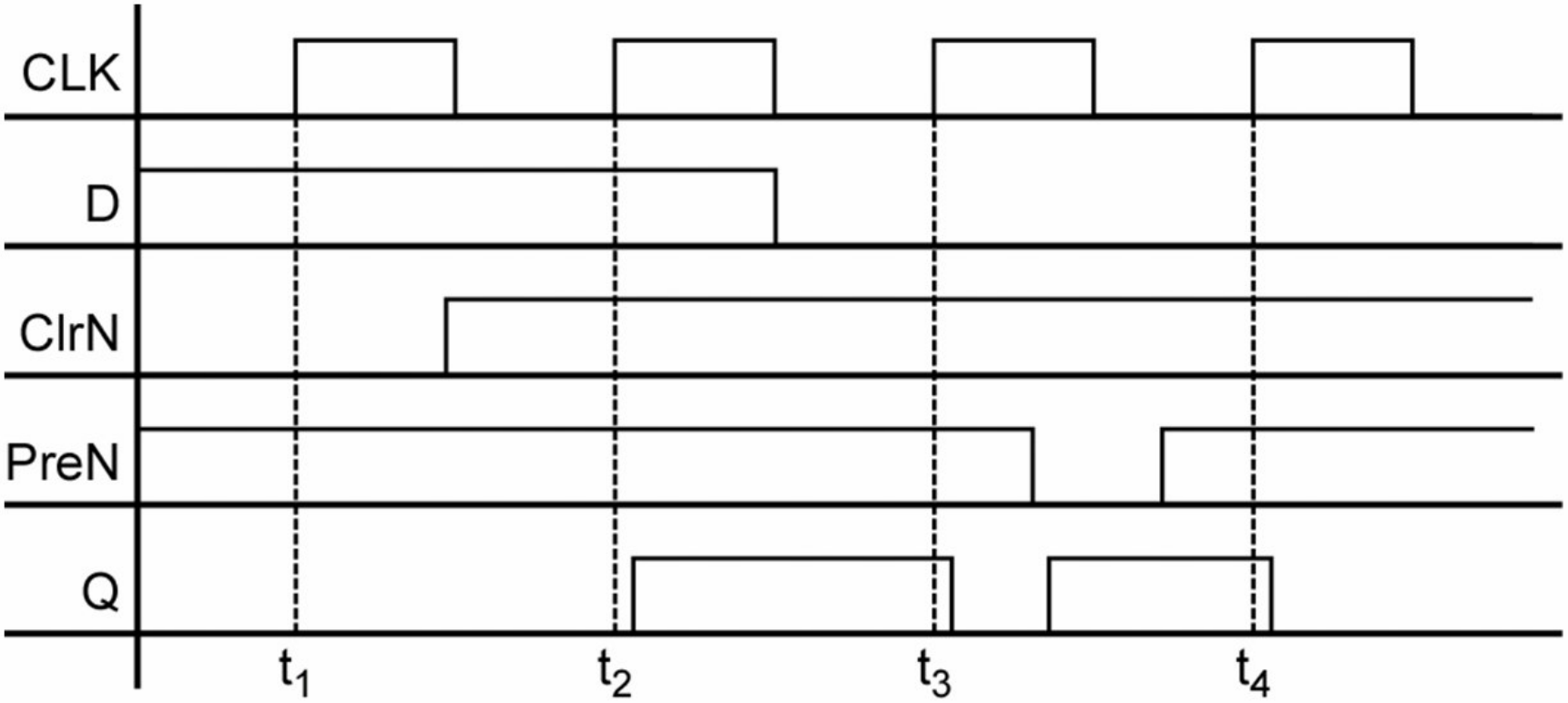


Figure 11-26: **Timing Diagram for D Flip-Flop with Asynchronous Clear and Preset**

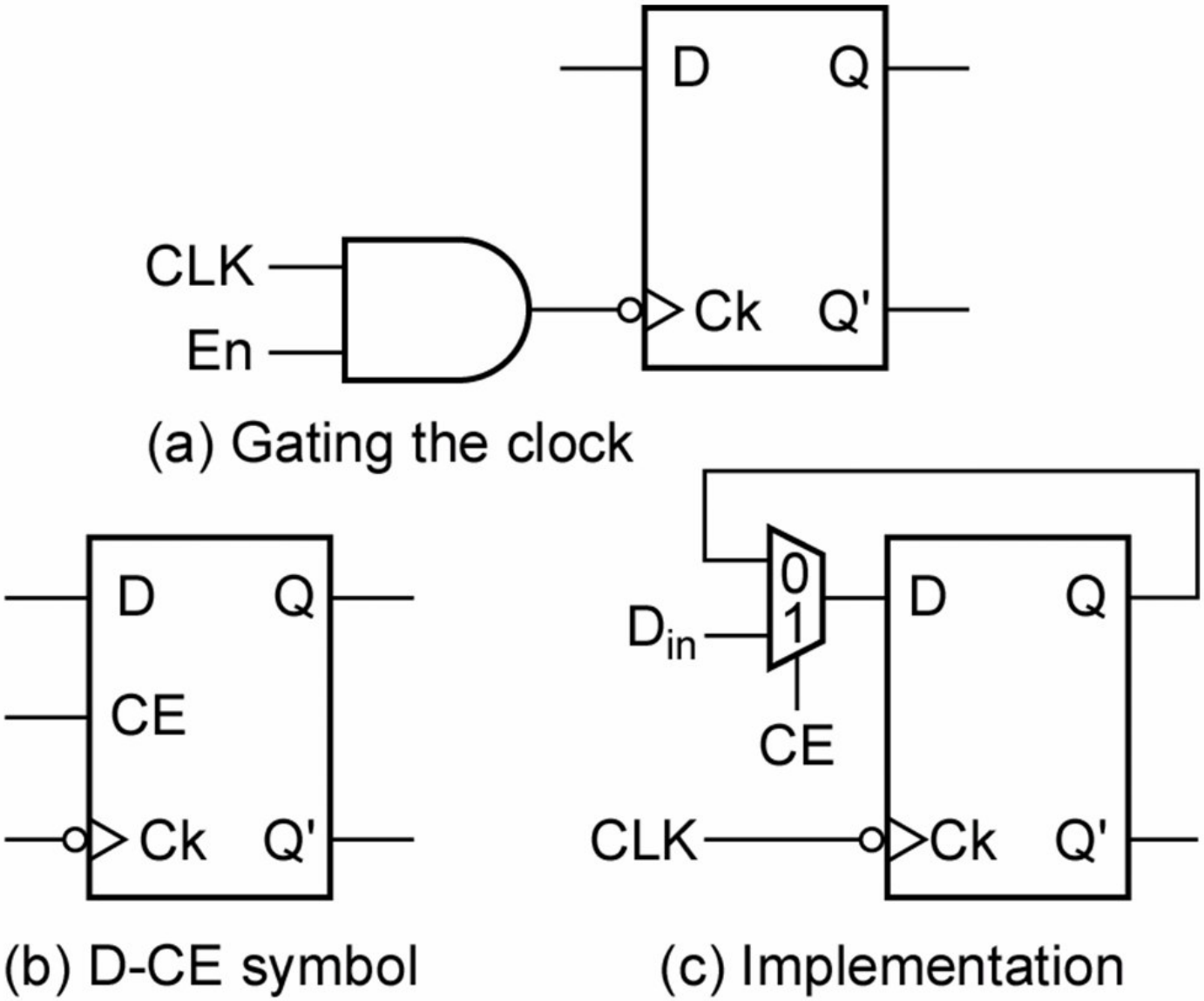


Figure 11-27: **D Flip-Flop with Clock Enable**